CHAPTER 5

Bipolar Junction Transistors (BJTs)

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INTRODUCTION

In this chapter, we study the other major three-terminal device: the bipolar junction transistor (BJT). The presentation of the material in this chapter parallels but does not rely on that for the MOSFET in Chapter 4; thus, if desired, the BJT can be studied before the MOSFET.

Three-terminal devices are far more useful than two-terminal ones, such as the diodes studied in Chapter 3, because they can be used in a multitude of applications, ranging from signal amplification to the design of digital logic and memory circuits. The basic principle involved is the use of the voltage between two terminals to control the current flowing in the third terminal. In this way, a three-terminal device can be used to realize a controlled source, which as we learned in Chapter 1 is the basis for amplifier design. Also, in the extreme, the control signal can be used to cause the current in the third terminal to change from zero to a large value, thus allowing the device to act as a switch. As we learned also in Chapter 1,
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the switch is the basis for the realization of the logic inverter, the basic element of digital circuits.

The invention of the BJT in 1948 at the Bell Telephone Laboratories ushered in the era of solid-state circuits, which led to electronics changing the way we work, play, and indeed, live. The invention of the BJT also eventually led to the dominance of information technology and the emergence of the knowledge-based economy.

The bipolar transistor enjoyed nearly three decades as the device of choice in the design of both discrete and integrated circuits. Although the MOSFET had been known very early on, it was not until the 1970s and 1980s that it became a serious competitor to the BJT. At the time of this writing (2003), the MOSFET is undoubtedly the most widely used electronic device, and CMOS technology is the technology of choice in the design of integrated circuits. Nevertheless, the BJT remains a significant device that excels in certain applications. For instance, the reliability of BJT circuits under severe environmental conditions makes them the dominant device in automotive electronics, an important and still-growing area.

The BJT remains popular in discrete circuit design, in which a very wide selection of BJT types are available to the designer. Here we should mention that the characteristics of the bipolar transistor are so well understood that one is able to design transistor circuits whose performance is remarkably predictable and quite insensitive to variations in device parameters. The BJT is still the preferred device in very demanding analog circuit applications, both integrated and discrete. This is especially true in very-high-frequency applications, such as radio frequency (RF) circuits for wireless systems. A very-high-speed digital logic-circuit family based on bipolar transistors, namely emitter-coupled logic, is still in use. Finally, bipolar transistors can be combined with MOSFETs to create innovative circuits that take advantage of the high-input-impedance and low-power operation of MOSFETs and the very-high-frequency operation and high-current-driving capability of bipolar transistors. The resulting technology is known as BiMOS or BiCMOS, and it is finding increasingly larger areas of application (see Chapters 6, 7, 10, and 11).

In this chapter, we shall start with a simple description of the physical operation of the BJT. Though simple, this physical description provides considerable insight regarding the performance of the transistor as a circuit element. We then quickly move from describing current flow in terms of electrons and holes to a study of the transistor terminal characteristics. Circuit models for transistor operation in different modes will be developed and utilized in the analysis and design of transistor circuits. The main objective of this chapter is to develop in the reader a high degree of familiarity with the BJT. Thus, by the end of the chapter, the reader should be able to perform rapid first-order analysis of transistor circuits and to design single-stage transistor amplifiers and simple logic inverters.

5.1 DEVICE STRUCTURE AND PHYSICAL OPERATION

5.1.1 Simplified Structure and Modes of Operation

Figure 5.1 shows a simplified structure for the BJT. A practical transistor structure will be shown later (see also Appendix A, which deals with fabrication technology).

As shown in Fig. 5.1, the BJT consists of three semiconductor regions: the emitter region (n type), the base region (p type), and the collector region (n type). Such a transistor is called an npn transistor. Another transistor, a dual of the npn as shown in Fig. 5.2, has a p-type emitter, an n-type base, and a p-type collector and is appropriately called a pnp transistor.
A terminal is connected to each of the three semiconductor regions of a transistor, with the terminals labeled emitter (E), base (B), and collector (C).

The transistor consists of two pn junctions, the emitter–base junction (EBJ) and the collector–base junction (CBJ). Depending on the bias condition (forward or reverse) of each of these junctions, different modes of operation of the BJT are obtained, as shown in Table 5.1.

The active mode, which is also called forward active mode, is the one used if the transistor is to operate as an amplifier. Switching applications (e.g., logic circuits) utilize both the cutoff and the saturation modes. The reverse active (or inverse active) mode has very limited application but is conceptually important.

As we will see shortly, charge carriers of both polarities—that is, electrons and holes—participate in the current conduction process in a bipolar transistor, which is the reason for the name bipolar.

<table>
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<tr>
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<th>CBJ</th>
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<td>Reverse</td>
<td>Reverse</td>
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<tr>
<td>Active</td>
<td>Forward</td>
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<td>Reverse active</td>
<td>Reverse</td>
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5.1.2 Operation of the npn Transistor in the Active Mode

Let us start by considering the physical operation of the transistor in the active mode. This situation is illustrated in Fig. 5.3 for the npn transistor. Two external voltage sources (shown as batteries) are used to establish the required bias conditions for active-mode operation. The voltage $V_{BE}$ causes the p-type base to be higher in potential than the n-type emitter, thus forward-biasing the emitter–base junction. The collector–base voltage $V_{CB}$ causes the n-type collector to be higher in potential than the p-type base, thus reverse-biasing the collector–base junction.

**Current Flow**

In the following description of current flow only diffusion-current components are considered. Drift currents due to thermally generated minority carriers are usually very small and can be neglected. Nevertheless, we will have more to say about these reverse-current components at a later stage.

The forward bias on the emitter–base junction will cause current to flow across this junction. Current will consist of two components: electrons injected from the emitter into the base, and holes injected from the base into the emitter. As will become apparent shortly, it is highly desirable to have the first component (electrons from emitter to base) at a much higher level than the second component (holes from base to emitter). This can be accomplished by fabricating the device with a heavily doped emitter and a lightly doped base; that is, the device is designed to have a high density of electrons in the emitter and a low density of holes in the base.

The current that flows across the emitter–base junction will constitute the emitter current $i_E$, as indicated in Fig. 5.3. The direction of $i_E$ is “out” of the emitter lead, which is in the direction of the hole current and opposite to the direction of the electron current, with the emitter current $i_E$ being equal to the sum of these two components. However, since the electron component is much larger than the hole component, the emitter current will be dominated by the electron component.

FIGURE 5.3  Current flow in an npn transistor biased to operate in the active mode. (Reverse current components due to drift of thermally generated minority carriers are not shown.)

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The material in this section assumes that the reader is familiar with the operation of the pn junction under forward-bias conditions (Section 3.X).
Let us now consider the electrons injected from the emitter into the base. These electrons will be minority carriers in the p-type base region. Because the base is usually very thin, in the steady state the excess minority carrier (electron) concentration in the base will have an almost straight-line profile, as indicated by the solid straight line in Fig. 5.4. The electron concentration will be highest [denoted by \( n_p(0) \)] at the emitter side and lowest (zero) at the collector side. As in the case of any forward-biased \( pn \) junction (Section 3.X), the concentration will be proportional to

\[
\frac{\frac{n_p(0)}{e^{\frac{V_{BE}}{V_T}}}}{W} = \frac{n_p(0)}{W}
\]

where \( n_p(0) \) is the thermal equilibrium value of the minority-carrier (electron) concentration in the base region, \( V_{BE} \) is the forward base–emitter bias voltage, and \( V_T \) is the thermal voltage, which is equal to approximately 25 mV at room temperature. The reason for the zero concentration at the collector side of the base is that the positive collector voltage \( V_{CB} \) causes the electrons at that end to be swept across the CBJ depletion region.

The tapered minority-carrier concentration profile (Fig. 5.4) causes the electrons injected into the base to diffuse through the base region toward the collector. This electron diffusion current \( I_e \) is directly proportional to the slope of the straight-line concentration profile,

\[
I_e = A_eqD_n \left( \frac{d n_p(x)}{dx} \right)
\]

\[
= A_eqD_n \left( \frac{n_p(0)}{W} \right)
\]

This minority carrier distribution in the base results from the boundary conditions imposed by the two junctions. It is not an exponentially decaying distribution, which would result if the base region were infinitely thick. Rather, the thin base causes the distribution to decay linearly. Furthermore, the reverse bias on the collector–base junction causes the electron concentration at the collector side of the base to be zero.
where $A_e$ is the cross-sectional area of the base–emitter junction (in the direction perpendicular to the page), $q$ is the magnitude of the electron charge, $D_n$ is the electron diffusivity in the base, and $W$ is the effective width of the base. Observe that the negative slope of the minority-carrier concentration results in a negative current $I_n$ across the base; that is, $I_n$ flows from right to left (in the negative direction of $x$).

Some of the electrons that are diffusing through the base region will combine with holes, which are the majority carriers in the base. However, since the base is usually very thin, the proportion of electrons “lost” through this recombination process will be quite small. Nevertheless, the recombination in the base region causes the excess minority-carrier concentration profile to deviate from a straight line and take the slightly concave shape indicated by the broken line in Fig. 5.4. The slope of the concentration profile at the EBJ is slightly higher than that at the CBJ, with the difference accounting for the small number of electrons lost in the base region through recombination.

The Collector Current

From the above we see that most of the diffusing electrons will reach the boundary of the collector–base depletion region. Because the collector is more positive than the base (by $V_{CB}$ volts), these successful electrons will be swept across the CBJ depletion region into the collector. They will thus get “collected” to constitute the collector current $i_C$. Thus $i_C = I_n$, which will yield a negative value for $i_C$, indicating that $i_C$ flows in the negative direction of the $x$ axis (i.e., from right to left). Since we will take this to be the positive direction of $i_C$, we can drop the negative sign in Eq. (5.2). Doing this and substituting for $n_i(0)$ from Eq. (5.1), we can thus express the collector current $i_C$ as

$$i_C = I_S e^{qV_{BE}/VT}$$

where the saturation current $I_S$ is given by

$$I_S = A_e q D_n n_i(0)/W$$

Substituting $n_i(0) = n_i^0/N_A$, where $n_i$ is the intrinsic carrier density and $N_A$ is the doping concentration of the base, we can express $I_S$ as

$$I_S = A_e q D_n n_i^0 N_A/W$$

An important observation to make here is that the magnitude of $i_C$ is independent of $V_{CB}$. That is, as long as the collector is positive with respect to the base, the electrons that reach the collector side of the base region will be swept into the collector and register as collector current.

The saturation current $I_S$ is inversely proportional to the base width $W$ and is directly proportional to the area of the EBJ. Typically $I_S$ is in the range of $10^{-12}$ A to $10^{-15}$ A (depending on the size of the device). Because $I_S$ is proportional to $n_i^0$, it is a strong function of temperature, approximately doubling for every 5°C rise in temperature. (For the dependence of $n_i^0$ on temperature, refer to Eq. 3.X.)

Since $I_S$ is directly proportional to the junction area (i.e., the device size), it will also be referred to as the scale current. Two transistors that are identical except that one has an EBJ area, say, twice that of the other will have saturation currents with that same ratio (i.e., 2). Thus for the same value of $V_{BE}$ the larger device will have a collector current twice that in the smaller device. This concept is frequently employed in integrated-circuit design.
The Base Current The base current $i_B$ is composed of two components. The first component $i_{B1}$ is due to the holes injected from the base region into the emitter region. This current component is proportional to $e^{eV_{BE}/V_T}$,

$$i_{B1} = \frac{AqD_np^2}{N_pL_p} e^{eV_{BE}/V_T}$$  \hspace{1cm} (5.5)

where $D_n$ is the hole diffusivity in the emitter, $L_p$ is the hole diffusion length in the emitter, and $N_p$ is the doping concentration of the emitter.

The second component of base current, $i_{B2}$, is due to holes that have to be supplied by the external circuit in order to replace the holes lost from the base through the recombination process. An expression for $i_{B2}$ can be found by noting that if the average time for a minority electron to recombine with a majority hole in the base is denoted $\tau_B$ (called minority-carrier lifetime), then in $\tau_B$ seconds the minority-carrier charge in the base, $Q_n$, recombines with holes. Of course in the steady state, $Q_n$ is replenished by electron injection from the emitter. To replenish the holes, the current $i_{B2}$ must supply the base with a positive charge equal to $Q_n$ every $\tau_B$ seconds,

$$i_{B2} = \frac{Q_n}{\tau_B}$$  \hspace{1cm} (5.6)

The minority-carrier charge stored in the base region, $Q_n$, can be found by reference to Fig. 5.4. Specifically, $Q_n$ is represented by the area of the triangle under the straight-line distribution in the base, thus

$$Q_n = Aqx \frac{1}{2} n_p(0) W$$

Substituting for $n_p(0)$ from Eq. (5.1) and replacing $n_p(0)$ by $n_p^0 / N_A$ gives

$$Q_n = \frac{AqWn_p^2}{2N_A} e^{eV_{BE}/V_T}$$  \hspace{1cm} (5.7)

which can be substituted in Eq. (5.6) to obtain

$$i_{B2} = \frac{1}{2} AqWn_p^2 e^{eV_{BE}/V_T}$$  \hspace{1cm} (5.8)

Combining Eqs. (5.5) and (5.8) and utilizing Eq. (5.4), we obtain for the total base current $i_B$ the expression

$$i_B = I_B \left( \frac{D_n N_p W}{D_p N_p^0 L_p} + \frac{1}{2D_n \tau_B} \right) e^{eV_{BE}/V_T}$$  \hspace{1cm} (5.9)

Comparing Eqs. (5.3) and (5.9), we see that $i_B$ can be expressed as a fraction of $i_C$ as follows:

$$i_B = \frac{I_B}{I_C} e^{eV_{BE}/V_T}$$  \hspace{1cm} (5.10)

That is,

$$i_B = \left( \frac{1}{\beta} \right) e^{eV_{BE}/V_T}$$  \hspace{1cm} (5.11)

where $\beta$ is given by

$$\beta = \frac{1}{\beta} \left( \frac{D_n N_p W}{D_p N_p^0 L_p} + \frac{1}{2D_n \tau_B} \right)$$  \hspace{1cm} (5.12)
from which we see that $\beta$ is a constant for the particular transistor. For modern npn transistors, $\beta$ is in the range 100 to 200, but it can be as high as 1000 for special devices. For reasons that will become clear later, the constant $\beta$ is called the common-emitter current gain.

Equation (5.12) indicates that the value of $\beta$ is highly influenced by two factors: the width of the base region, $W$, and the relative dopings of the base region and the emitter region, $(N_e/N_B)$. To obtain a high $\beta$ (which is highly desirable since $\beta$ represents a gain parameter) the base should be thin ($W$ small) and lightly doped and the emitter heavily doped $(N_e/N_B$ small). Finally, we note that the discussion thus far assumes an idealized situation, where $\beta$ is a constant for a given transistor.

The Emitter Current

Since the current that enters a transistor must leave it, it can be seen from Fig. 5.3 that the emitter current $i_E$ is equal to the sum of the collector current $i_C$ and the base current $i_B$,

$$i_E = i_C + i_B$$  \hspace{1cm} (5.13)

Use of Eqs. (5.10) and (5.13) gives

$$i_E = \beta + \frac{1}{\beta} i_C$$  \hspace{1cm} (5.14)

That is,

$$i_E = \beta + \frac{1}{\beta} i_C e^{-v_B/e_V}$$  \hspace{1cm} (5.15)

Alternatively, we can express Eq. (5.14) in the form

$$i_C = \alpha i_E$$  \hspace{1cm} (5.16)

where the constant $\alpha$ is related to $\beta$ by

$$\alpha = \frac{\beta}{\beta + 1}$$  \hspace{1cm} (5.17)

Thus the emitter current in Eq. (5.15) can be written

$$i_E = (1/\alpha) e^{-v_B/e_V}$$  \hspace{1cm} (5.18)

Finally, we can use Eq. (5.17) to express $\beta$ in terms of $\alpha$; that is,

$$\beta = \frac{\alpha}{1 - \alpha}$$  \hspace{1cm} (5.19)

It can be seen from Eq. (5.17) that $\alpha$ is a constant (for the particular transistor) that is less than but very close to unity. For instance, if $\beta = 100$, then $\alpha \approx 0.99$. Equation (5.19) reveals an important fact: Small changes in $\alpha$ correspond to very large changes in $\beta$. This mathematical observation manifests itself physically, with the result that transistors of the same type may have widely different values of $\beta$. For reasons that will become apparent later, $\alpha$ is called the common-base current gain.

Finally, we should note that because $\alpha$ and $\beta$ characterize the operation of the BJT in the “forward active” mode, as opposed to the “reverse active” mode, which we shall discuss shortly, they are often denoted $\alpha_F$ and $\beta_F$. We shall use $\alpha$ and $\alpha_F$ interchangeably and, similarly, $\beta$ and $\beta_F$. 


We have presented a first-order model for the operation of the \( npn \) transistor in the active (or “forward” active) mode. Basically, the forward-bias voltage \( v_{BE} \) causes an exponentially related current \( i_C \) to flow in the collector terminal. The collector current \( i_C \) is independent of the value of the collector voltage as long as the collector–base junction remains reverse-biased; that is, \( v_{CB} \geq 0 \). Thus in the active mode the collector terminal behaves as an ideal constant-current source where the value of the current is determined by \( v_{BE} \). The base current \( i_B \) is a factor of the collector current, and the emitter current is equal to the sum of the collector and base currents. Since \( i_B \) is much smaller than \( i_C \), \( \frac{i_B}{i_C} \approx \frac{1}{\beta} \). More precisely, the collector current is a fraction \( \alpha_F \) of the emitter current, with \( \alpha_F \) smaller than, but close to, unity.

This first-order model of transistor operation in the forward active mode can be represented by the equivalent circuit shown in Fig. 5.5(a). Here diode \( D_E \) has a scale current \( I_{SE} \) equal to \( i_C \) and thus provides a current \( i_E \) related to \( v_{BE} \) according to Eq. (5.18). The current of the controlled source, which is equal to the collector current, is controlled by \( v_{BE} \) according to the exponential relationship indicated, a restatement of Eq. (5.3). This model is in essence a nonlinear voltage-controlled current source. It can be converted to the current-controlled current-source model shown in Fig. 5.5(b) by expressing the current of the controlled source as \( \alpha_F i_E \). Note that this model is also nonlinear because of the exponential relationship of the current \( i_E \) through diode \( D_E \) and the voltage \( v_{BE} \). From this model we observe that if the transistor is used as a two-port network with the input port between \( E \) and \( B \) and the output port between \( C \) and \( B \) (i.e., with \( B \) as a common terminal), then the current gain observed is equal to \( \alpha_E \). This \( \alpha_E \) is called the common-base current gain.

**EXERCISES**

5.1 Consider an \( npn \) transistor with \( v_{BE} = 0.7 \) V at \( i_C = 1 \) mA. Find \( v_{BE} \) at \( i_C = 0.1 \) mA and 10 mA.

_Ans._ 0.64 V; 0.76 V
5.1.3 Structure of Actual Transistors

Figure 5.6 shows a more realistic (but still simplified) cross-section of an npn BJT. Note that the collector virtually surrounds the emitter region, thus making it difficult for the electrons injected into the thin base to escape being collected. In this way, the resulting $\alpha_F$ is close to unity and $\beta_F$ is large. Also, observe that the device is not symmetrical. For more details on the physical structure of actual devices, the reader is referred to Appendix A.

The fact that the BJT structure is not symmetrical means that if the emitter and collector are interchanged and the transistor is operated in the reverse active mode, the resulting values of $\alpha$ and $\beta$, denoted $\alpha_R$ and $\beta_R$, will be different from the forward active mode values, $\alpha_F$ and $\beta_F$. Furthermore, because the structure is optimized for forward mode operation, $\alpha_R$ and $\beta_R$ will be much lower than their forward mode counterparts. Of course, $\alpha_R$ and $\beta_R$ are related by equations identical to those that relate $\alpha_F$ and $\beta_F$. Typically, $\alpha_R$ is in the range of 0.01 to 0.5, and the corresponding range of $\beta_R$ is 0.01 to 1.

The structure in Fig. 5.6 indicates also that the CBJ has a much larger area than the EBJ. It follows that if the transistor is operated in the reverse active mode (i.e., with the CBJ forward biased and the EBJ reverse biased) and the operation is modeled in the manner of Fig. 5.5(b), we obtain the model shown in Fig. 5.7. Here diode DC represents the collector-base junction and has a scale current $I_{SC}$ that is much larger than the scale current $I_{SE}$ of diode DE. The two scale currents have, of course, the same ratio as the areas of the corresponding junctions. Furthermore, a simple and elegant formula relates the scale currents $I_{SE}$, $I_{SC}$, and $I_e$ and the current gains $\alpha_F$ and $\alpha_R$, namely

$$\alpha_F I_{SE} = \alpha_R I_{SC} = I_e$$  \hspace{1cm} (5.20)

**FIGURE 5.6** Cross-section of an npn BJT.
5.1 DEVICE STRUCTURE AND PHYSICAL OPERATION

The large scale current $I_{SC}$ has the effect that for the same current, the CBJ exhibits a lower voltage drop when forward biased than the forward voltage drop of the EBJ, $V_{BE}$. This point will have implications for the BJT’s operation in the saturation mode.

5.1.4 The Ebers-Moll (EM) Model

The model of Fig. 5.5(a) can be combined with that of Fig. 5.7 to obtain the circuit model shown in Fig. 5.8. Note that we have relabelled the currents through $D_E$ and $D_C$ and the corresponding control currents of the controlled sources as $I_{DE}$ and $I_{DC}$. Ebers and Moll, two

EXERCISE

5.5 A particular transistor is said to have $a_E = 1$ and $a_I = 0.01$. Its emitter scale current ($I_{SE}$) is approximately $10^{-15}$ A. What is its collector scale current ($I_{SC}$)? What is the size of the collector junction relative to the emitter junction? What is the value of $\beta$?

Ans. $10^{-13}$ A; 100 times larger; 0.01

FIGURE 5.7 Model for the npn transistor when operated in the reverse active mode (i.e., with the CBJ forward biased and the EBJ reverse biased).

FIGURE 5.8 The Ebers-Moll (EM) model of the npn transistor.
early workers in the area, have shown that this composite model can be used to predict the operation of the BJT in all of its possible modes. To see how this can be done, we derive expressions for the terminal currents \( i_E \), \( i_C \), and \( i_B \) in terms of the junction voltages \( v_{BE} \) and \( v_{BC} \). Toward that end, we write an expression for the current at each of the three nodes of the model in Fig. 5.8 as follows:

\[
\begin{align*}
i_E &= i_{DE} - \alpha_j i_{DC} \\
i_C &= -i_{DE} + \alpha_j i_{DC} \\
i_B &= (1 - \alpha_j) i_{DE} + (1 - \alpha_R) i_{DC}
\end{align*}
\]

(5.21) (5.22) (5.23)

Then we use the diode equation to express \( i_{DE} \) and \( i_{DC} \) as

\[
\begin{align*}
i_{DE} &= I_{SE} e^{v_{BE}/V_T} - 1 \\
i_{DC} &= I_{SC} e^{v_{BC}/V_T} - 1
\end{align*}
\]

(5.24) (5.25)

Substituting for \( i_{DE} \) and \( i_{DC} \) into Eqs. (5.21), (5.22), and (5.23) and using the relationship in Eq. (5.20) yield the required expressions:

\[
\begin{align*}
i_E &= I_E e^{v_{BE}/V_T} - 1 - I_D (e^{v_{BC}/V_T} - 1) \\
i_C &= I_C (e^{v_{BE}/V_T} - 1) - I_D (e^{v_{BC}/V_T} - 1) \\
i_B &= I_B (e^{v_{BE}/V_T} - 1) + (1 - \beta_R) (e^{v_{BC}/V_T} - 1)
\end{align*}
\]

(5.26) (5.27) (5.28)

where

\[
\begin{align*}
\beta_E &= \frac{\alpha_j}{1 - \alpha_j} \\
\beta_R &= \frac{\alpha_R}{1 - \alpha_R}
\end{align*}
\]

(5.29) (5.30)

As a first application of the EM model, we shall use it to predict the terminal currents of a transistor operating in the forward active mode. Here \( v_{BE} \) is positive and in the range of 0.6 V to 0.8 V, and \( v_{BC} \) is negative. One can easily see that terms containing \( e^{v_{BC}/V_T} \) will be negligibly small and can be neglected to obtain

\[
\begin{align*}
i_E &= I_E e^{v_{BE}/V_T} + I_D (1 - 1/\alpha_j) \\
i_C &= I_C e^{v_{BE}/V_T} + I_D (1 - 1/\alpha_R) \\
i_B &= I_B e^{v_{BE}/V_T} - I_D (1 + 1/\beta_R)
\end{align*}
\]

(5.31) (5.32) (5.33)
In each of these three equations, one can normally neglect the second term on the right-hand side. This results in the familiar current-voltage relationships we derived earlier, namely, Eqs. (5.18), (5.3), and (5.11), respectively.

Thus far, we have stated the condition for forward active mode operation as $v_{CB} \geq 0$ to ensure that the CBJ is reverse biased. In actual fact, however, a $pn$ junction does not become effectively forward biased until the forward voltage across it exceeds approximately 0.5 V or so. It follows that one can maintain active mode operation of an $nnp$ transistor for negative $v_{CB}$ down to approximately –0.4 V or so. This is illustrated in Fig. 5.9, which shows a sketch of $i_C$ versus $v_{CB}$ for an $nnp$ transistor operated with a constant emitter current $I_E$. Observe that $i_C$ remains constant at $\alpha F I_E$ for $v_{CB}$ going negative to approximately –0.4 V. Below this value of $v_{CB}$, the CBJ becomes forward biased and the transistor leaves the active mode and enters the saturation mode of operation, where $i_C$ decreases. We shall study BJT saturation next. For now, however, note that we can use the EM equations to verify that the terms containing $e^{v_{BC}/V_T}$ remain negligibly small for $v_{BC}$ as high as 0.4 V.

### Exercise 5.6
For a BJT with $\alpha_F = 0.99$, $\alpha_R = 0.02$, and $I_S = 10^{-15}$ A, calculate the second term on the right-hand side of each of Eqs. (5.31), (5.32), and (5.33) to verify that they can be ignored. Then calculate $i_E$, $i_C$, and $i_B$ for $v_{BE} = 0.7$ V.

**Ans.** $-10^{-17}$ A; $49 \times 10^{-15}$ A; $-3 \times 10^{-17}$ A; 1.461 mA; 1.446 mA; 0.0145 mA

### 5.1.5 Operation in the Saturation Mode
Figure 5.9 indicates that as $v_{CB}$ is lowered below approximately 0.4 V, the BJT enters the saturation mode of operation. Ideally, $v_{CB}$ has no effect on the collector current in the active mode, but the situation changes dramatically in saturation: Increasing $v_{CB}$ in the negative direction—that is, increasing the forward-bias voltage of the CBJ—reduces $i_C$. To see this analytically, consider the Ebers-Moll expression for $i_C$ in Eq. (5.27) and, for simplicity, neglect the terms not involving exponentials to obtain

$$i_C = I_C e^{v_{BE}/V_T} - \frac{I_E}{\alpha R} e^{v_{BC}/V_T}$$

(5.34)

The first term on the right-hand side is a result of the forward-biased EBJ, and the second term is a result of the forward-biased CBJ. The second term starts to play a role when $v_{BC}$ exceeds approximately 0.4 V or so. As $v_{BC}$ is increased, this term becomes larger and subtracts from the first term, causing $i_C$ to reduce, eventually reaching zero. Of course, one can operate

---

*Saturation in a BJT means something completely different from that in a MOSFET. The saturation mode of operation of the BJT is analogous to the triode region of operation of the MOSFET. On the other hand, the saturation region of operation of the MOSFET corresponds to the active mode of BJT operation.*
the saturated transistor at any value of $i_C$ lower than $\alpha F_\text{IE}$. We will have more to say about saturation-mode operation in subsequent sections. Here, however, it is instructive to examine the minority-carrier concentration profile in the base of the saturated transistor, as shown in Fig. 5.10. Observe that because the CBJ is now forward biased, the electron concentration at the collector edge of the base is no longer zero; rather, it is a value proportional to $\alpha F_\text{IE}$. Also note that the slope of the concentration profile is reduced in correspondence with the reduction in $i_C$. 

**FIGURE 5.9** The $i_C$–$v_{CB}$ characteristics of an npn transistor fed with a constant emitter current $I_E$. The transistor enters the saturation mode of operation for $v_{CB} < -0.4 \text{ V}$, and the collector current falls off.

**FIGURE 5.10** Concentration profile of the minority carriers (electrons) in the base of an npn transistor operating in saturation mode.
5.1.6 The pnp Transistor

The pnp transistor operates in a manner similar to that of the npn device described above. Figure 5.11 shows a pnp transistor biased to operate in the active mode. Here the voltage $V_{EB}$ causes the p-type emitter to be higher in potential than the n-type base, thus forward-biasing the base–emitter junction. The collector–base junction is reverse-biased by the voltage $V_{BC}$, which keeps the p-type collector lower in potential than the n-type base.

Unlike the npn transistor, current in the pnp device is mainly conducted by holes injected from the emitter into the base as a result of the forward-bias voltage $V_{EB}$. Since the component of emitter current contributed by electrons injected from base to emitter is kept small by using a lightly doped base, most of the emitter current will be due to holes. The electrons injected from base to emitter give rise to the first component of base current, $i_{B1}$. Also, a number of the holes injected into the base will recombine with the majority carriers (electrons) and will thus be lost. The disappearing base electrons will have to be replaced from the external circuit, giving rise to the second component of base current, $i_{B2}$.

The holes that succeed in reaching the boundary of the depletion region of the collector–base junction will be attracted by the negative voltage on the collector. Thus these holes will be swept across the depletion region into the collector and appear as collector current.

EXERCISE

5.7 (a) Use the EM expressions in Eqs. (5.26) and (5.27) to show that the $i_C–v_{CB}$ relationship sketched in Fig. 5.9 can be described by $i_C = \frac{\alpha_F I_E}{\alpha_F - (1/\alpha_R)} e^{v_{BC}/V_T}$. Neglect all terms not containing exponentials.

(b) For the case $I_C = 10^{-15}$ A, $I_E = 1$ mA, $\alpha_F = 1$, and $\alpha_R = 0.01$, find $i_C$ for $v_{BC} = -1$ V, +0.4 V, +0.5 V, and +0.57 V. Also find the value of $v_{BC}$ at which $i_C = 0$.

(c) At the value of $v_{BC}$ that makes $i_C$ zero, what do you think $i_B$ should be? Verify using Eq. (5.28).

Ans. 1 mA; 1 mA; 0.95 mA; 0.76 mA; 0.20 mA; 576 mV; 1 mA; 1 mA.

5.1.6 The pnp Transistor

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The holes that succeed in reaching the boundary of the depletion region of the collector–base junction will be attracted by the negative voltage on the collector. Thus these holes will be swept across the depletion region into the collector and appear as collector current.

FIGURE 5.11 Current flow in a pnp transistor biased to operate in the active mode.
It can easily be seen from the above description that the current-voltage relationships of the \textit{pnp} transistor will be identical to those of the \textit{npn} transistor except that $v_{BE}$ has to be replaced by $v_{EB}$. Also, the large-signal active-mode operation of the \textit{pnp} transistor can be modeled by the circuit depicted in Fig. 5.12. As in the \textit{npn} case, another version of this equivalent circuit is possible in which the current source is replaced with a current-controlled current source $\alpha F_i E$. Finally, we note that the \textit{pnp} transistor can operate in the saturation mode in a manner analogous to that described for the \textit{npn} device.

5.2 CURRENT-VOLTAGE CHARACTERISTICS

5.2.1 Circuit Symbols and Conventions

The physical structure used thus far to explain transistor operation is rather cumbersome to employ in drawing the schematic of a multitransistor circuit. Fortunately, a very descriptive and convenient circuit symbol exists for the BJT. Figure 5.13(a) shows the symbol for the \textit{npn} transistor; the \textit{pnp} symbol is given in Fig. 5.13(b). In both symbols the emitter is distinguished by an arrowhead. This distinction is important because, as we have seen in the last section, practical BJTs are not symmetric devices.

The polarity of the device—\textit{npn} or \textit{pnp}—is indicated by the direction of the arrowhead on the emitter. This arrowhead points in the direction of normal current flow in the emitter, which is also the forward direction of the base-emitter junction. Since we have adopted a
drawing convention by which currents flow from top to bottom, we will always draw pnp transistors in the manner shown in Fig. 5.13 (i.e., with their emitters on top).

Figure 5.14 shows npn and pnp transistors biased to operate in the active mode. It should be mentioned in passing that the biasing arrangement shown, utilizing two dc sources, is not a usual one and is used merely to illustrate operation. Practical biasing schemes will be presented in Section 5.5. Figure 5.14 also indicates the reference and actual directions of current flow throughout the transistor. Our convention will be to take the reference direction to coincide with the normal direction of current flow. Hence, normally, we should not encounter a negative value for \( i_E \), \( i_B \), or \( i_C \).

The convenience of the circuit drawing convention that we have adopted should be obvious from Fig. 5.14. Note that currents flow from top to bottom and that voltages are higher at the top and lower at the bottom. The arrowhead on the emitter also implies the polarity of the emitter–base voltage that should be applied in order to forward bias the emitter–base junction. Just a glance at the circuit symbol of the pnp transistor, for example, indicates that we should make the emitter higher in voltage than the base (by \( V_{EB} \)) in order to cause current to flow into the emitter (downward). Note that the symbol \( V_{EB} \) means the voltage by which the emitter (E) is higher than the base (B). Thus for a pnp transistor operating in the active mode \( V_{EB} \) is positive, while in an npn transistor \( V_{BE} \) is positive.

From the discussion of Section 5.1 it follows that an npn transistor whose EBJ is forward biased will operate in the active mode as long as the collector voltage does not fall below that of the base by more than approximately 0.4 V. Otherwise, the transistor leaves the active mode and enters the saturation region of operation.
In a parallel manner, the pnp transistor will operate in the active mode if the EBJ is forward biased and the collector voltage is not allowed to rise above that of the base by more than 0.4 V or so. Otherwise, the CBJ becomes forward biased, and the pnp transistor enters the saturation region of operation.

For easy reference, we present in Table 5.2 a summary of the BJT current-voltage relationships in the active mode of operation. Note that for simplicity we use $\alpha$ and $\beta$ rather than $\alpha_F$ and $\beta_F$.

The Constant $n$ In the diode equation (Chapter 3) we used a constant $n$ in the exponential and mentioned that its value is between 1 and 2. For modern bipolar junction transistors the constant $n$ is close to unity except in special cases: (1) at high currents (i.e., high relative to the normal current range of the particular transistor) the $i_C$–$v_{BE}$ relationship exhibits a value for $n$ that is close to 2, and (2) at low currents the $i_B$–$v_{BE}$ relationship shows a value for $n$ of approximately 2. Note that for our purposes we shall assume always that $n = 1$.

The Collector–Base Reverse Current ($I_{CBO}$) In our discussion of current flow in transistors we ignored the small reverse currents carried by thermally generated minority carriers. Although such currents can be safely neglected in modern transistors, the reverse current across the collector–base junction deserves some mention. This current, denoted $I_{CBO}$, is the reverse current flowing from collector to base with the emitter open-circuited (hence the subscript $O$). This current is usually in the nanoampere range, a value that is many times higher than its theoretically predicted value. As with the diode reverse current, $I_{CBO}$ contains a substantial leakage component, and its value is dependent on $v_{CB}$. $I_{CBO}$ depends strongly on temperature, approximately doubling for every 10°C rise.\(^5\)

\(^5\)The temperature coefficient of $I_{CBO}$ is different from that of $I_C$ because $I_{CBO}$ contains a substantial leakage component.
EXAMPLE 5.1

The transistor in the circuit of Fig. 5.15(a) has $\beta = 100$ and exhibits a $v_{BE}$ of 0.7 V at $i_C = 1$ mA. Design the circuit so that a current of 2 mA flows through the collector and a voltage of +5 V appears at the collector.

Solution

Refer to Fig. 5.15(b). We note at the outset that since we are required to design for $V_C = +5$ V, the CBJ will be reverse biased and the BJT will be operating in the active mode. To obtain a voltage $V_C = +5$ V the voltage drop across $R_C$ must be $15 - 5 = 10$ V. Now, since $i_C = 2$ mA, the value of $R_C$ should be selected according to

$$R_C = \frac{10 \text{ V}}{2 \text{ mA}} = 5 \text{ k}\Omega$$

Since $v_{BE} = 0.7$ V at $i_C = 1$ mA, the value of $v_{BE}$ at $i_C = 2$ mA is

$$V_{BE} = 0.7 + V_T \ln \left( \frac{2}{1} \right) = 0.717 \text{ V}$$

Since the base is at 0 V, the emitter voltage should be

$$V_E = -0.717 \text{ V}$$

For $\beta = 100$, $\alpha = 100/101 = 0.99$. Thus the emitter current should be

$$I_E = \frac{i_C}{\alpha} = \frac{2}{0.99} = 2.02 \text{ mA}$$

Now the value required for $R_E$ can be determined from

$$R_E = \frac{V_E - (-15)}{I_E} = \frac{-0.717 + 15}{2.02} = 7.07 \text{ k}\Omega$$
This completes the design. We should note, however, that the calculations above were made with a
degree of accuracy that is usually neither necessary nor justified in practice in view, for instance, of
the expected tolerances of component values. Nevertheless, we chose to do the design precisely in
order to illustrate the various steps involved.

**EXERCISES**

5.10 In the circuit shown in Fig. E5.10, the voltage at the emitter was measured and found to be –0.7 V. If
\( \beta = 50 \), find \( I_E \), \( I_B \), \( I_C \), and \( V_C \).

**FIGURE E5.10**

\[ V_C \]

\[ V_E \]

\[ V_B \]

\[ +10 \text{ V} \]

\[ 5 \text{k}\Omega \]

\[ -10 \text{ V} \]

\[ 10 \text{k}\Omega \]

\[ J_E \]

\[ J_B \]

\[ \text{Ans.} 0.93 \text{ mA}; 18.2 \mu\text{A}; 0.91 \text{ mA}; +5.45 \text{ V} \]

5.11 In the circuit shown in Fig. E5.11, measurement indicates \( V_B \) to be +1.0 V and \( V_E \) to be +1.7 V. What
are \( \alpha \) and \( \beta \) for this transistor? What voltage \( V_C \) do you expect at the collector?

**FIGURE E5.11**

\[ V_C \]

\[ V_B \]

\[ V_E \]

\[ +10 \text{ V} \]

\[ 5 \text{k}\Omega \]

\[ -10 \text{ V} \]

\[ 100 \text{k}\Omega \]

\[ 5 \text{k}\Omega \]

\[ \text{Ans.} 0.994; 165; -1.75 \text{ V} \]
5.2.2 Graphical Representation of Transistor Characteristics

It is sometimes useful to describe the transistor $i-v$ characteristics graphically. Figure 5.16 shows the $i_C-v_{BE}$ characteristic, which is the exponential relationship

$$i_C = I_S e^{\frac{v_{BE}}{\frac{1}{n}V_T}}$$

which is identical (except for the value of constant $n$) to the diode $i-v$ relationship. The $i_C-v_{BE}$ and $i_E-v_{BE}$ characteristics are also exponential but with different scale currents: $I_S/e$ for $i_C$ and $I_S/B$ for $i_E$. Since the constant of the exponential characteristic, $1/V_T$, is quite high ($=40$), the curve rises very sharply. For $v_{BE}$ smaller than about 0.5 V, the current is negligibly small. Also, over most of the normal current range $v_{BE}$ lies in the range of 0.6 V to 0.8 V. In performing rapid first-order dc calculations we normally will assume $V_{BE} \approx 0.7$ V, which is similar to the approach used in the analysis of diode circuits (Chapter 3). For a $pnp$ transistor, the $i_C-v_{BE}$ characteristic will look identical to that of Fig. 5.16.

As in silicon diodes, the voltage across the emitter–base junction decreases by about 2 mV for each rise of 1°C in temperature, provided that the junction is operating at a constant current. Figure 5.17 illustrates this temperature dependence by depicting $i_C-v_{BE}$ curves at three different temperatures for an $npn$ transistor.

The Common-Base Characteristics

One way to describe the operation of a transistor is to plot $i_C$ versus $v_{CB}$ for various values of $i_E$. We have already encountered one such graph, in Fig. 5.9, which we used to introduce the saturation mode of operation. A conceptual experimental setup for measuring such characteristics is shown in Fig. 5.18(a). Observe that in these measurements the base voltage is held constant, here at ground potential, and thus the base serves as a common terminal between the input and output ports. Consequently, the resulting set of characteristics, shown in Fig. 5.18(b), are known as common-base characteristics.

---

5 The $i_C-v_{BE}$ characteristic is the BJT’s counterpart of the $i_D-v_{GS}$ characteristic of the enhancement MOSFET. They share an important attribute: In both cases the voltage has to exceed a “threshold” for the device to conduct appreciably. In the case of the MOSFET, there is a formal threshold voltage, $V_T$, which lies in the range of 0.6 V to 0.8 V. For the BJT, there is an “apparent threshold” of approximately 0.5 V. The $i_D-v_{GS}$ characteristic of the MOSFET is parabolic and thus is less steep than the $i_C-v_{BE}$ characteristic of the BJT. This difference has a direct and significant implication to the value of transconductance $g_m$, realized with each device.
In the active region of operation, obtained for \( V_{CB} \) or so, the \( i_C - v_{CB} \) curves deviate from our expectations in two ways. First, the curves are not horizontal straight lines but show a small positive slope, indicating that \( i_C \) depends slightly on \( v_{CB} \) in the active mode. We shall discuss this phenomenon shortly. Second, at relatively large values of \( v_{CB} \), the collector current shows a rapid increase, which is a breakdown phenomenon we will consider at a later stage.

As indicated in Fig. 5.18(b), each of the characteristic curves intersects the vertical axis at a current level equal to \( \alpha I_E \), where \( I_E \) is the constant emitter current at which the particular curve is measured. The resulting value of \( \alpha \) is a total or large-signal \( \alpha \), that is, \( \alpha = i_C / i_E \), where \( i_C \) and \( i_E \) denote total collector and emitter currents, respectively. Here we recall that \( \alpha \) is appropriately called the common-base current gain. An incremental or small-signal \( \alpha \) can be determined by measuring the change in \( i_C \), \( \Delta i_C \), obtained as a result of changing \( i_E \) by an increment \( \Delta i_E \), \( \alpha = \Delta i_C / \Delta i_E \). This measurement is usually made at a constant \( v_{CB} \), as indicated in Fig. 5.18(b). Usually, the values of incremental and total \( \alpha \) differ slightly, but we shall not make a distinction between the two in this book.

**FIGURE 5.17** Effect of temperature on the \( i_C - v_{BE} \) characteristic. At a constant emitter current (broken line), \( v_{BE} \) changes by \( \sim 2 \) mV/°C.

**FIGURE 5.18** The \( i_C - v_{CB} \) characteristics for an npn transistor.
Finally, turning to the saturation region, the Ebers-Moll equations can be used to obtain the following expression for the $i_C - v_{CB}$ curve in the saturation region (for $i_E = I_E$),

$$i_C = \alpha_F I_E - \frac{1}{\alpha_R} \left( \frac{1}{\alpha_R} \right) e^{v_{BC}/V_T} \quad (5.35)$$

We can use this equation to determine the value of $v_{BC}$ at which $i_C$ is reduced to zero. Recall that the CBJ is much larger than the EBJ, the forward-voltage drop $v_{BC}$ will be smaller than $v_{BE}$ resulting in a collector-emitter voltage, $v_{CE}$, of 0.1 V to 0.3 V in saturation.

### EXERCISES

5.12 Consider a pnp transistor with $v_{BE} = 0.7$ V at $i_E = 1$ mA. Let the base be grounded, the emitter be fed by a 2-mA constant-current source, and the collector be connected to a -5-V supply through a 1-kΩ resistor. If the temperature increases by 30°C, find the changes in emitter and collector voltages. Neglect the effect of $i_{CBO}$.

**Ans.** -60 mV; 0 V.

5.13 Find the value of $v_{BC}$ at which $i_C$ of an npn transistor operated in the CB configuration with $I_E = 1$ mA is reduced (a) to half its active-mode value and (b) to zero. Assume $\alpha_F = 1$ and $\alpha_R = 0.1$. The value of $V_{BE}$ was measured for $v_{CB} = 0$ [see measuring setup in Fig. 5.18(a)] and found to be 0.70 V. Repeat (a) and (b) for $\alpha_R = 0.01$.

**Ans.** 0.628 V; 0.645 V; 0.568 V; 0.585 V.

### 5.2.3 Dependence of $i_C$ on the Collector Voltage—The Early Effect

When operated in the active region, practical BJTs show some dependence of the collector current on the collector voltage, with the result that their $i_C - v_{CE}$ characteristics are not perfectly horizontal straight lines. To see this dependence more clearly, consider the conceptual circuit shown in Fig. 5.19(a). The transistor is connected in the common-emitter configuration; that is, here the emitter serves as a common terminal between the input and output ports. The voltage $V_{CE}$ can be set to any desired value by adjusting the dc source connected between base and emitter. At each value of $V_{BE}$, the corresponding $i_C - v_{CE}$ characteristic curve can be measured point-by-point by varying the dc source connected between collector and emitter and measuring the corresponding collector current. The result is the family of $i_C - v_{CE}$ characteristic curves shown in Fig. 5.19(b) and known as common-emitter characteristics.

At low values of $v_{CE}$, as the collector voltage goes below that of the base by more than 0.4 V, the collector-base junction becomes forward biased and the transistor leaves the active mode and enters the saturation mode. We shall shortly look at the details of the $i_C - v_{CE}$ curves in the saturation region. At this time, however, we wish to examine the characteristic curves in the active region in detail. We observe that the characteristic curves, though still straight lines, have finite slope. In fact, when extrapolated, the characteristic lines meet at a point on the negative $v_{CE}$ axis, at $v_{CE} = -V_A$. The voltage $V_A$, a positive number, is a parameter for the particular BJT, with typical values in the range of 50 V to 100 V. It is called the Early voltage, after J. M. Early, the engineering scientist who first studied this phenomenon.

At a given value of $v_{CE}$, increasing $v_{CE}$ increases the reverse-bias voltage on the collector-base junction and thus increases the width of the depletion region of this junction (refer to Fig. 5.3). This in turn results in a decrease in the effective base width $W$. Recalling that $I_E$ is inversely proportional to $W$ (Eq. 5.4), we see that $I_E$ will increase and that $i_C$ increases proportionally. This is the Early effect.
The linear dependence of $i_C$ on $v_{CE}$ can be accounted for by assuming that $I_S$ remains constant and including the factor $(1 + v_{CE}/V_A)$ in the equation for $i_C$ as follows:

$$i_C = I_S e^{v_{BE}/V_T} \left(1 + v_{CE}/V_A\right)$$  \hfill (5.36)

The nonzero slope of the $i_C - v_{CE}$ straight lines indicates that the output resistance looking into the collector is not infinite. Rather, it is finite and defined by

$$r_o = \left|\frac{\partial i_C}{\partial v_{CE}}\right|_{i_C, V_{BE\text{ constant}}}$$  \hfill (5.37)

Using Eq. (5.36) we can show that

$$r_o = \frac{V_A + V_{CE}}{I_C}$$  \hfill (5.38)

where $I_C$ and $V_{CE}$ are the coordinates of the point at which the BJT is operating on the particular $i_C - v_{CE}$ curve (i.e., the curve obtained for $V_{BE} = V_{BE\text{ constant}}$). Alternatively, we can write

$$r_o = \frac{V}{I_C}$$  \hfill (5.38a)

where $I_C$ is the value of the collector current with the Early effect neglected; that is,

$$I_C' = I_C e^{v_{BE}/V_T}$$  \hfill (5.38b)

It is rarely necessary to include the dependence of $i_C$ on $v_{CE}$ in dc bias design and analysis. However, the finite output resistance $r_o$ can have a significant effect on the gain of transistor amplifiers, as will be seen in later sections and chapters.

The output resistance $r_o$ can be included in the circuit model of the transistor. This is illustrated in Fig. 5.20, where we show large-signal circuit models of a common-emitter npn transistor operating in the active mode. Observe that diode $D_0$ models the exponential dependence of $i_B$ on $v_{BE}$ and thus has a scale current $I_{EB0} = I_f/\beta$. Also note that the two models
5.2 CURRENT-VOLTAGE CHARACTERISTICS

5.2.4 The Common-Emitter Characteristics

An alternative way of expressing the transistor common-emitter characteristics is illustrated in Fig. 5.21. Here the base current $i_b$ rather than the base–emitter voltage $v_{BE}$ is used as a parameter. That is, each $i_c-v_{CE}$ curve is measured with the base fed with a constant current $i_b$. The resulting characteristics look similar to those in Fig. 5.19 except that here we show the breakdown phenomenon, which we shall discuss shortly. We should also mention that although it is not obvious from the graphs, the slope of the curves in the active region of operation differs from the corresponding slope in Fig. 5.19. This, however, is a rather subtle point and beyond our interest at this moment.

EXERCISES

5.14 Find the output resistance of a BJT for which $V_A = 100$ V at $I_C = 0.1, 1,$ and 10 mA.

Ans. 1 MΩ; 100 kΩ; 10 kΩ

5.15 Consider the circuit in Fig. 5.19(a). At $V_{CE} = 1$ V, $V_{BE}$ is adjusted to yield a collector current of 1 mA. Then, while $V_{BE}$ is kept constant, $V_{CE}$ is raised to 11 V. Find the new value of $I_C$. For this transistor, $V_A = 100$ V.

Ans. 1.1 mA

5.2.4 The Common-Emitter Characteristics

An alternative way of expressing the transistor common-emitter characteristics is illustrated in Fig. 5.21. Here the base current $i_b$ rather than the base–emitter voltage $v_{BE}$ is used as a parameter. That is, each $i_c-v_{CE}$ curve is measured with the base fed with a constant current $i_b$. The resulting characteristics look similar to those in Fig. 5.19 except that here we show the breakdown phenomenon, which we shall discuss shortly. We should also mention that although it is not obvious from the graphs, the slope of the curves in the active region of operation differs from the corresponding slope in Fig. 5.19. This, however, is a rather subtle point and beyond our interest at this moment.

The Common-Emitter Current Gain $\beta$ An important transistor parameter is the common-emitter current gain $\beta$, or simply $\beta$. Thus far we have defined $\beta$ as the ratio of the total current in the collector to the total current in the base, and we have assumed that $\beta$ is constant for a given transistor, independent of the operating conditions. In the following we examine those two points in some detail.

Consider a transistor operating in the active region at the point labeled $Q$ in Fig. 5.21, that is, at a collector current $I_{CQ}$, a base current $I_{BQ}$, and a collector-emitter voltage $V_{CEQ}$. The


The ratio of the collector current to the base current is the **large-signal or dc** $\beta$, which is the $\beta$ we have been using in our description of transistor operation. It is commonly referred to on the manufacturer’s data sheets as $h_{FE}$, a symbol that comes from the use of the hybrid, or $h$, two-port parameters to characterize transistor operation (see Appendix X and Appendix Y). One can define another $\beta$ based on incremental or small-signal quantities.

Referring to Fig. 5.21 we see that while keeping $v_{CE}$ constant at the value $V_{CEQ}$, changing $i_B$ from $I_{BQ}$ to $(I_{BQ} + \Delta i_B)$ results in $i_C$ increasing from $I_{CQ}$ to $I_{CQ} + \Delta i_C$. Thus we can define the **incremental or ac** $\beta$, $\beta_{ac}$, as

\[
\beta_{ac} = \frac{\Delta i_C}{\Delta i_B} \quad \text{at } v_{CE} = \text{constant} \tag{5.40}
\]

The magnitudes of $\beta_{ac}$ and $\beta_{dc}$ differ, typically by approximately 10% to 20%. In this book we shall not normally make a distinction between the two. Finally, we should mention that the small-signal $\beta$ or $\beta_{ac}$ is also known by the alternate symbol $h_{fe}$. Because the small-signal $\beta$ or $h_{fe}$ is defined and measured at a constant $v_{CE}$—that is, with a zero signal component between collector and emitter—it is known as the **short-circuit common-emitter current gain**.

The value of $\beta$ depends on the current at which the transistor is operating and the relationship takes the form shown in Fig. 5.22. The physical processes that give rise to this relationship are beyond the scope of this book. Figure 5.22 also shows the temperature dependence of $\beta$.

**The Saturation Voltage** $V_{CEsat}$ and **Saturation Resistance** $R_{CESat}$. An expanded view of the common-emitter characteristics in the saturation region is shown in Fig. 5.23. The fact that the curves are “bunched” together in the saturation region implies that the incremental $\beta$ is lower than in the active region. A possible operating point in the saturation region is that labeled X. It is characterized by a base current $I_{B}$, a collector current $I_{Csat}$, and a collector–emitter voltage $V_{CEsat}$. Note that $I_{Csat} < \beta_{ac}I_{B}$ since the value of $I_{Csat}$ is decided on
5.2 CURRENT-VOLTAGE CHARACTERISTICS

by the circuit designer, a saturated transistor is said to be operating at a **forced** $\beta$ given by

$$\beta_{\text{forced}} = \frac{I_{C\text{sat}}}{I_B}$$

Thus,

$$\beta_{\text{forced}} < \beta_f$$

The ratio of $\beta_f$ to $\beta_{\text{forced}}$ is known as the **overdrive factor**. The greater the overdrive factor, the deeper the transistor is driven into saturation and the lower $V_{CE\text{sat}}$ becomes.
The $i_C-v_{CE}$ curves in saturation are rather steep, indicating that the saturated transistor exhibits a low collector-to-emitter resistance $R_{CE}^s$.

$$R_{CE}^s = \frac{\partial v_{CE}}{\partial i_C}$$  \hspace{1cm} (5.43)

Typically, $R_{CE}^s$ ranges from a few ohms to a few tens of ohms.

Figure 5.24(b) shows one of the $i_C-v_{CE}$ characteristic curves of the saturated transistor shown in Fig. 5.24(a). It is interesting to note that the curve intersects the $v_{CE}$ axis at $V_T \ln \alpha$, a value common to all the $i_C-v_{CE}$ curves. We have also shown in Fig. 5.24(b) the tangent at operating point X of slope $1/R_{CE}^s$. When extrapolated, the tangent intersects the $v_{CE}$-axis at a voltage $V_{CE}^o$, typically approximately 0.1 V. It follows that the $i_C-v_{CE}$ characteristic of a saturated transistor can be approximately represented by the equivalent circuit shown in Fig. 5.24(c). At the collector side, the transistor is represented by a resistance $R_{CE}^s$ in

![Image of transistor with circuit diagram]
series with a battery $V_{CE\text{off}}$. Thus the saturation voltage $V_{CE\text{sat}}$ can be found from

$$V_{CE\text{sat}} = V_{CE\text{off}} + I_{CE\text{sat}} R_{CE\text{sat}} \quad (5.44)$$

Typically, $V_{CE\text{sat}}$ falls in the range of 0.1 V to 0.3 V. For many applications the even simpler model shown in Fig. 5.24(d) suffices. The offset voltage of a saturated transistor, though small, makes the BJT less attractive as a switch than the MOSFET, whose $i_D - v_{DS}$ characteristics go right through the origin of the $i_D - v_{DS}$ plane.

It is interesting and instructive to use the Ebers-Moll model to derive analytical expressions for the characteristics of the saturated transistor. Toward that end we use Eqs. (5.28) and (5.27), substitute $I_B = I_B^*$, and neglect the small terms that do not include exponentials; thus,

$$I_C = I_B^* e^{v_{BE}/V_T} + I_F e^{v_{BC}/V_T} \quad (5.45)$$

$$I_C = I_C^* e^{v_{CE}/V_T} \quad (5.46)$$

Dividing Eq. (5.46) by Eq. (5.45) and writing $v_{BC} = v_{BE} + v_{CE}$ enables us to express $I_C$ in the form

$$I_C = \left( \frac{v_{CE}}{v_{BC}} \right)^* I_B^* \frac{e^{v_{BE}/V_T}}{e^{v_{BC}/V_T} + \beta} \quad (5.47)$$

This is the equation of the $I_C - V_{CE}$ characteristic curve obtained when the base is driven with a constant current $I_B$. Figure 5.25 shows a typical plot of the normalized collector current $I_C^*/(\beta I_B^*)$.

![Plot of the normalized $I_C$ versus $V_{CE}$ for an npn transistor with $\beta_F = 100$ and $\alpha_R = 0.1$.](image)
which is equal to \((\beta_{\text{sat}}/\beta_F)\) versus \(v_{CE}\). As shown, the curve can be approximated by a straight line coincident with the tangent at the point \(\beta_{\text{sat}}/\beta_F = 0.5\). It can be shown that this tangent has a slope of approximately 10 V\(^{-1}\), independent of the transistor parameters. Thus,

\[
R_{\text{CEsat}} = \frac{1}{1/10 \beta_F I_B}
\]

Other important parameters of the normalized plot are indicated in Fig. 5.25. Finally, we can obtain an expression for \(V_{CE}\) sat by substituting \(i_C = I_{\text{sat}}\) and \(v_{CE} = V_{CE}\) sat in Eq. (5.47),

\[
V_{CE}\sat = V_T \ln \left( \frac{1 + (\beta_{\text{sat}}/\beta_F) I_B}{1 - (\beta_{\text{sat}}/\beta_F)} \right)
\]

### EXERCISES

5.16 An npn transistor characterized by \(\beta_F = 100\) and \(\alpha_R = 0.1\) is operated in saturation with a constant base current of 0.1 mA and a forced \(\beta_F\) of 10. Find the values of \(V_{CE}\) at \(i_C = 0\), \(R_{CE}\sat\), and \(V_{CE}\off\). Use the latter two figures to obtain an approximate value for \(V_{CE}\sat\) [i.e., using the equivalent circuit model of Fig. 5.24(c)]. Find a more accurate value for \(V_{CE}\sat\) using Eq. (5.49), and compare results. Repeat for a \(\beta_F\) of 20.

**Ans.** 58 mV; 10 \(\Omega\); 120 mV; 130 mV and 118 mV; 140 mV and 137 mV.

5.17 Measurements made on a BJT operated in saturation with a constant base-current drive provide the following data: at \(i_C = 5\) mA, \(v_{CE} = 170\) mV; at \(i_C = 2\) mA, \(v_{CE} = 110\) mV. What are the values of the offset voltage \(V_{CE}\off\) and saturation resistance \(R_{CE}\sat\) in this situation?

**Ans.** 70 mV; 20 \(\Omega\).

### 5.2.5 Transistor Breakdown

The maximum voltages that can be applied to a BJT are limited by the EBJ and CBJ breakdown effects that follow the avalanche multiplication mechanism described in Section 3.X. Consider first the common-base configuration. The \(i_C-v_{CB}\) characteristics in Fig. 5.18(b) indicate that for \(i_E = 0\) (i.e., with the emitter open-circuited) the collector–base junction breaks down at a voltage denoted by \(B_{VCBO}\). For \(i_E > 0\), breakdown occurs at voltages smaller than \(B_{VCBO}\). Typically, \(B_{VCBO}\) is greater than 50 V.

Next consider the common-emitter characteristics of Fig. 5.21, which show breakdown occurring at a voltage \(B_{VCBO}\). Here, although breakdown is still of the avalanche type, the effects on the characteristics are more complex than in the common-base configuration. We will not explain these details; it is sufficient to point out that typically \(B_{VCBO}\) is about half \(B_{VCBO}\). On the transistor data sheets \(B_{VCBO}\) is sometimes referred to as the "sustaining voltage \(LV_{CE}\)."

Breakdown of the CBJ in either the common-base or common-emitter configuration is not destructive as long as the power dissipation in the device is kept within safe limits. This, however, is not the case with the breakdown of the emitter–base junction. The EBJ breaks down in an avalanche manner at a voltage \(B_{VCBO}\) much smaller than \(B_{VCBO}\). Typically, \(B_{VCBO}\) is in the range of 6 V to 8 V, and the breakdown is destructive in the sense that the \(\beta\) of the transistor is permanently reduced. This does not prevent use of the EBJ as a zener diode to generate reference voltages in IC design. In such applications, however, one is not concerned with the \(\beta\)-degradation effect. A circuit arrangement to prevent EBJ breakdown in IC amplifiers will be discussed in Chapter 10. Transistor breakdown and the maximum allowable power dissipation are important parameters in the design of power amplifiers (Chapter 9).
5.2 CURRENT-VOLTAGE CHARACTERISTICS

5.2.6 Summary
We conclude our study of the current-voltage characteristics of the BJT with a summary of important results in Table 5.3.

### TABLE 5.3 Summary of the BJT Current-Voltage Characteristics

<table>
<thead>
<tr>
<th>Circuit Symbol and Directions of Current Flow</th>
<th>npn Transistor</th>
<th>pnp Transistor</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image" alt="Diagram" /></td>
<td><img src="image" alt="Diagram" /></td>
<td><img src="image" alt="Diagram" /></td>
</tr>
</tbody>
</table>

**Operation in the Active Mode** *(for Amplifier Application)*

1. **EBJ Forward Biased**
   - $v_{BC} > V_{CEON} = 0.5 \text{ V}$
   - Typically, $v_{BE} = 0.7 \text{ V}$
   - $v_{CE} \leq V_{CEON} = 0.4 \text{ V}$
   - $v_{BE} \geq 0.3 \text{ V}$

2. **CBI Reversed Biased**
   - $v_{BE} > V_{BEON} = 0.5 \text{ V}$
   - Typically, $v_{BE} = 0.7 \text{ V}$
   - $v_{CE} \leq V_{CEON} = 0.4 \text{ V}$
   - $v_{BE} \geq 0.3 \text{ V}$

*(Continued)*
TABLE 5.3 (Continued)

<table>
<thead>
<tr>
<th>Current-Voltage Relationships</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$i_C = I_C e^{v_{BE}/V_T}$</td>
<td>$i_C = I_C e^{v_{CE}/V_A}$</td>
</tr>
<tr>
<td>$i_B = i_C / \beta \Rightarrow i_C = \beta i_B$</td>
<td></td>
</tr>
<tr>
<td>$i_E = i_C / \alpha \Rightarrow i_C = \alpha i_E$</td>
<td></td>
</tr>
<tr>
<td>$\beta = \frac{\alpha}{1 - \alpha} \Rightarrow \alpha = \frac{\beta}{\beta + 1}$</td>
<td></td>
</tr>
<tr>
<td>$\beta = \beta_T, \alpha = \alpha_T$</td>
<td></td>
</tr>
<tr>
<td>$i_T$ = Transistor scale current; proportional to EBJ area; doubles for every 5°C rise in temperature.</td>
<td></td>
</tr>
<tr>
<td>$V_T$ = Thermal voltage = $kT/q \approx 25$ mV at room temperature.</td>
<td></td>
</tr>
<tr>
<td>At a constant $i_T$, $</td>
<td>P_{out}</td>
</tr>
</tbody>
</table>

Large-Signal Equivalent-Circuit Model (Including the Early Effect)

\[
\begin{align*}
\frac{v_{BE}}{V_T} &= i_C I_S e^{v_{BE}/V_T} \\
\frac{v_{CE}}{V_A} &= i_C I_S e^{v_{CE}/V_A} \\
\end{align*}
\]

Ebers-Moll Model

\[
\begin{align*}
\frac{v_{BE}}{V_T} &= \frac{i_C}{i_B} I_S e^{v_{BE}/V_T} \\
\frac{v_{CE}}{V_A} &= \frac{i_C}{i_E} I_S e^{v_{CE}/V_A} \\
\end{align*}
\]
5.2 CURRENT-VOLTAGE CHARACTERISTICS

Operation in the Saturation Mode

**Conditions:**

1. EBJ Forward-Biased
   - \( v_{BE} > V_{BE} \) on;
   - \( V_{BE} \) on \( \approx 0.5 \text{ V} \)
   - Typically, \( v_{BE} = 0.7–0.8 \text{ V} \)

2. CBJ Forward-Biased
   - \( v_{BC} \geq V_{BC} \) on;
   - \( V_{BC} \) on \( \approx 0.4 \text{ V} \)
   - Typically, \( v_{BC} = 0.5–0.6 \text{ V} \)

\[ v_{CE} = V_{CE}^{\text{sat}} = 0.1–0.2 \text{ V} \]

\[ v_{EB} > V_{EB} \] on;
- Typically, \( v_{EB} = 0.7–0.8 \text{ V} \)

\[ v_{CB} \geq V_{CB} \] on;
- Typically, \( v_{CB} = 0.5–0.6 \text{ V} \)

\[ v_{EC} = V_{EC}^{\text{sat}} = 0.1–0.2 \text{ V} \]

**Currents**

\[ i_{c} = \beta_{\text{forced}} i_{b} \]

\[ \beta_{\text{forced}} = \beta_{f} \]

**Equivalent Circuits**

\[ V_{CE}^{\text{sat}} + \beta \cdot \frac{i_{b}}{\beta_{\text{forced}}^2} = V_{C} \]

\[ R_{CE}^{\text{sat}} = 1/10 \beta_{f} i_{b} \]

\[ V_{CE}^{\text{sat}} = V_{b} \ln \left[ \frac{(\beta_{\text{forced}} + 1)/\beta_{f}}{1 - \beta_{\text{forced}}/\beta_{f}} \right] \]
5.3 THE BJT AS AN AMPLIFIER AND AS A SWITCH

Having studied the terminal characteristics of the BJT, we are now ready to consider its two major areas of application: as a signal amplifier, and as a digital-circuit switch. The basis for the amplifier application is that when the BJT is operated in the active mode, it acts as a voltage-controlled current source: Changes in the base–emitter voltage \(v_{BE}\) give rise to changes in the collector current \(i_C\). Thus in the active mode the BJT can be used to implement a transconductance amplifier (see Section 1.5). Voltage amplification can be obtained simply by passing the collector current through a resistance \(RC\), as will be seen shortly.

Since we are particularly interested in linear amplification, we will have to devise a way to achieve it in the face of the highly nonlinear behavior of the transistor, namely, that the collector current \(i_C\) is exponentially related to \(v_{BE}\). We will use the approach described in general terms in Section 1.4. Specifically, we will bias the transistor to operate at a dc base–emitter voltage \(V_{BE}\) and a corresponding dc collector current \(I_C\). Then we will superimpose the signal to be amplified, \(v_{be}\), on the dc voltage \(V_{BE}\). By keeping the amplitude of the signal \(v_{be}\) small, we will be able to constrain the transistor to operate on a short, almost linear segment of the \(i_C–v_{BE}\) characteristic; thus, the change in collector current, \(i_C\), will be linearly related to \(v_{be}\). We will study the small-signal operation of the BJT later in this section and in greater detail in Section 5.5. First, however, we will look at the “big picture.” We will study the total or large-signal operation of a BJT amplifier. From the transfer characteristic of the circuit, we will be able to see clearly the region over which the circuit can be operated as a linear amplifier. We also will be able to see how the BJT can be employed as a switch.

5.3.1 Large-Signal Operation—The Transfer Characteristic

Figure 5.26(a) shows the basic structure (skeleton) of the most commonly used BJT amplifier, the grounded-emitter or common-emitter (CE) circuit. The total input voltage \(v_I\) (bias + signal) is applied between base and emitter; that is, \(v_{BE} = v_I\). The total output voltage \(v_O\) (bias + signal) is taken between collector and ground; that is, \(v_{CE} = v_O\). Resistor \(RC\) has two functions: to establish a desired dc bias voltage at the collector, and to convert the collector signal current \(i_C\) to an output voltage, \(v_{CE}\) or \(v_O\). The supply voltage \(V_{CC}\) is needed to bias the BJT as well as to supply the power needed for the operation of the amplifier.

Figure 5.26(b) shows the voltage transfer characteristic of the CE circuit of Fig. 5.26(a). To understand how this characteristic arises, we first express \(v_O\) as

\[
v_O = v_{CE} = V_{CC} - R_C i_C
\]

Next, we observe that since \(v_{BE} = v_I\), the transistor will be effectively cutoff for \(v_I < 0.5\) V or so. Thus, for the range \(0 < v_I < 0.5\) V, \(i_C\) will be negligibly small, and \(v_O\) will be equal to the supply voltage \(V_{CC}\) (segment XY of the transfer curve).

As \(v_I\) is increased above 0.5 V, the transistor begins to conduct, and \(i_C\) increases. From Eq. (5.50), we see that \(v_O\) decreases. However, since initially \(v_I\) will be large, the BJT will

---

3 An introduction to amplifiers from an external-terminals point of view was presented in Sections 1.4 and 1.5, and it would be helpful for readers who are not familiar with basic amplifier concepts to review this material before proceeding with the study of BJT amplifiers.
be operating in the active mode, which gives rise to the sharply descending segment YZ of
the voltage transfer curve. The equation for this segment can be obtained by substituting in
Eq. (5.50) the active-mode expression for $i_C$, namely,

$$i_C = I_S e^{v_{BE}/V_T}$$

$$= I_S e^{v_{BE}/V_T}$$

where we have, for simplicity, neglected the Early effect. Thus we obtain

$$v_O = V_{CC} - R_C I_S e^{v_{BE}/V_T} \quad (5.51)$$

We observe that the exponential term in this equation gives rise to the steep slope of the YZ
segment of the transfer curve. Active-mode operation ends when the collector voltage ($v_O$ or $v_{CE}$)
falls by 0.4 V or so below that of the base ($v_{BE}$). At this point, the CBJ turns on, and the transistor enters the saturation region. This is indicated by point Z on the transfer curve. Observe that further increases in $v_{BE}$ cause $v_{CE}$ to decrease only slightly: In the saturation region, $v_{CE} = V_{CE\text{sat}}$ which falls in the narrow range of 0.1 V to 0.2 V. It is the almost-constant $V_{CE\text{sat}}$ that gives this region of BJT operation the name saturation. The collector current will also remain nearly constant at the value $I_{C\text{sat}}$.

$$I_{C\text{sat}} = \frac{V_{CC} - V_{CE\text{sat}}}{R_{C}}$$  \hspace{1cm} (5.52)

We recall from our study of the saturation region of operation in the previous section that the saturated BJT exhibit a very small resistance $R_{CE\text{sat}}$ between its collector and emitter. Thus, when saturated, the transistor in Fig. 5.26 provides a low-resistance path between the collector node C and ground and hence can be thought of as a closed switch. On the other hand, when the BJT is cutoff, it conducts negligibly small (ideally zero) current and thus acts as an open switch, effectively disconnecting node C from ground. The status of the switch (i.e., open or closed) is determined by the value of the control voltage $v_{BE}$. Very shortly, we will show that the BJT switch can also be controlled by the base current.

### 5.3.2 Amplifier Gain

To operate the BJT as a linear amplifier, it must be biased at a point in the active region. Figure 5.26(b) shows such a bias point, labeled Q (for quiescent point), and characterized by a dc base–emitter voltage $V_{BE}$ and a dc collector–emitter voltage $V_{CE}$. If the collector current at this value of $V_{BE}$ is denoted $I_C$, that is,

$$I_C = I_{Se} v_{BE}/v_T$$  \hspace{1cm} (5.53)

then from the circuit in Fig. 5.26(a) we can write

$$V_{CE} = V_{CC} - R_C I_C$$  \hspace{1cm} (5.54)

Now, if the signal to be amplified, $v_i$, is superimposed on $V_{BE}$ and kept sufficiently small, as indicated in Fig. 5.26(b), the instantaneous operating point will be constrained to a relatively short, almost-linear segment of the transfer curve around the bias point Q. The slope of this linear segment will be equal to the slope of the tangent to the transfer curve at Q. This slope is the voltage gain of the amplifier for small-input signals around Q. An expression for the small-signal gain $A_v$ can be found by differentiating the expression in Eq. (5.51) and evaluating the derivative at point Q; that is, for $v_i = V_{BE}$,

$$A_v = \frac{dV_{CE}}{dv_i} \bigg|_{v_i = V_{BE}}$$  \hspace{1cm} (5.55)

Thus,

$$A_v = -\frac{1}{V_T} I_{Se} v_{BE}/v_T R_C$$

Now, using Eq. (5.53) we can express $A_v$ in compact form:

$$A_v = -\frac{I_{Se} R_C}{V_T} = -\frac{V_{CE}}{V_T}$$  \hspace{1cm} (5.56)
5.3 THE BJT AS AN AMPLIFIER AND AS A SWITCH

where $V_{RC}$ is the dc voltage drop across $R_C$.

\[ V_{RC} = V_{CC} - V_{CE} \]  
(5.57)

Observe that the CE amplifier is inverting; that is, the output signal is 180° out of phase relative to the input signal. The simple expression in Eq. (5.56) indicates that the voltage gain of the common-emitter amplifier is the ratio of the dc voltage drop across $R_C$ to the thermal voltage $V_T$ (≈ 25 mV at room temperature). It follows that to maximize the voltage gain we should use as large a voltage drop across $R_C$ as possible. For a given value of $V_{CC}$, Eq. (5.57) indicates that to increase $V_{RC}$, we have to operate at a lower $V_{CE}$. However, reference to Fig. 5.26(b) shows that a lower $V_{CE}$ means a bias point Q close to the end of the active-region segment, which might not leave sufficient room for the negative-output signal swing without the amplifier entering the saturation region. If this happens, the negative peaks of the waveform of $v_o$ will be clipped off. Indeed, it is the need to allow sufficient room for output signal swing that determines the placement of the bias point Q on the active-region segment, YZ, of the transfer curve. Placing Q too high on this segment not only results in reduced gain (because $V_{CC}$ is lower) but could possibly limit the allowable range of positive signal swing. At this end, the limitation is imposed by the BJT cutting off, in which event the positive-output peaks would be clipped off at a level equal to $V_{CC}$.

Finally, it is useful to note that the theoretical maximum gain $A_v$ is obtained by biasing the BJT at the edge of saturation, which of course would not leave any room for negative signal swing. The resulting gain is given by

\[ A_v = \frac{V_{CE} - V_{CE_{sat}}}{V_T} \]  
(5.58)

Thus,

\[ A_{v\text{max}} = \frac{V_{CC} - V_{CE_{sat}}}{V_T} \]  
(5.59)

Although the gain can be increased by using a larger supply voltage, other considerations come into play when determining an appropriate value for $V_{CC}$. In fact, the trend has been toward using lower and lower supply voltages, currently approaching 1 V or so. At such low supply voltages, large gain values can be obtained by replacing the resistance $R_C$ with a constant-current source, as will be seen in Chapter 6.

EXAMPLE 5.2

Consider a common-emitter circuit with a BJT having $I_S = 10^{-15}$ A, a collector resistance $R_C = 6.8 \text{k} \Omega$, and a power supply $V_{CC} = 10$ V.

(a) Determine the value of the bias voltage $V_{BE}$ required to operate the transistor at $V_{CE} = 3.2$ V. What is the corresponding value of $I_E$?

(b) Find the voltage gain $A_v$ at this bias point. If an input sine-wave signal of 5-mV peak amplitude is superimposed on $V_{BE}$, find the amplitude of the output sine-wave signal (assume linear operation).

(c) Find the positive increment in $v_{BE}$ (above $V_{BE}$) that drives the transistor to the edge of saturation with $v_{CE} = 0.3$ V.
(d) Find the negative increment in $v_{BE}$ that drives the transistor to within 1% of cutoff (i.e., $v_o = 0.99V_{CC}$).

**Solution**

(a) 

\[ I_c = \frac{V_{CC} - V_{CE}}{R_C} \]

\[ = \frac{10 - 3.2}{6.8} = 1 \text{ mA} \]

The value of $V_{BE}$ can be determined from

\[ 1 \times 10^{-3} = 10^{-15} e^{V_{BE}/V_T} \]

which results in

\[ V_{BE} = 690.8 \text{ mV} \]

(b) 

\[ A_v = \frac{V_{CE} - V_{CE}'}{V_T} \]

\[ = \frac{10 - 3.2}{0.025} = -272 \text{ V/V} \]

\[ \dot{V}_{oc} = 272 \times 0.005 = 1.36 \text{ V} \]

(c) For $v_{BE} = 0.3 \text{ V}$,

\[ i_c = \frac{10 - 0.3}{6.8} = 1.617 \text{ mA} \]

To increase $i_c$ from 1 mA to 1.617 mA, $v_{BE}$ must be increased by

\[ \Delta v_{BE} = V_T \ln \left( \frac{1.617}{1} \right) \]

\[ = 12 \text{ mV} \]

(d) For $v_o = 0.99V_{CC} = 9.9 \text{ V}$,

\[ i_c = \frac{10 - 9.9}{6.8} = 0.0147 \text{ mA} \]

To decrease $i_c$ from 1 mA to 0.0147 mA, $v_{BE}$ must change by

\[ \Delta v_{BE} = V_T \ln \left( \frac{0.0147}{1} \right) \]

\[ = -105.5 \text{ mV} \]
5.3.3 Graphical Analysis

Although formal graphical methods are of little practical value in the analysis and design of most transistor circuits, it is illustrative to portray graphically the operation of a simple transistor amplifier circuit. Consider the circuit of Fig. 5.27, which is similar to the circuit we have been studying except for an added resistance in the base lead, $R_B$. A graphical analysis of the operation of this circuit can be performed as follows: First, we have to determine the dc bias point. Toward that end we set $v_i = 0$ and use the technique illustrated in Fig. 5.28 to determine the dc base current $I_B$. We next move to the $i_C−v_{CE}$ characteristics, shown in Fig. 5.29. We know that the operating point will lie on the $i_C−v_{CE}$ curve corresponding to

EXERCISE

5.19 While keeping $I_C$ unchanged at 1 mA, find the value of $R_C$ that will result in a voltage gain of $-320$ V/V. What is the largest negative signal swing allowed at the output (assume that $v_{CE}$ is not to decrease below 0.3 V)? What approximately is the corresponding input signal amplitude? (Assume linear operation).

Ans. 8 kΩ; 1.7 V; 5.3 mV

5.20 For the circuit of Fig. 5.27, find the maximum positive swing allowed at the output before the transistor enters the active region. (Assume linear operation. In other words, $v_{CE}$ never decreases below 0.3 V).

Ans. 12 V

FIGURE 5.27 Circuit whose operation is to be analyzed graphically.

FIGURE 5.28 Graphical construction for the determination of the dc base current in the circuit of Fig. 5.27.
the value of base current we have determined (the curve for $i_B = I_B$). Where it lies on the curve will be determined by the collector circuit. Specifically, the collector circuit imposes the constraint

$$v_{CE} = V_{CC} - i_C R_C$$

which can be rewritten as

$$i_C = \frac{V_{CC} - V_{CE}}{R_C}$$

which represents a linear relationship between $v_{CE}$ and $i_C$. This relationship can be represented by a straight line, as shown in Fig. 5.29. Since $R_C$ can be considered the amplifier load, the straight line of slope $-1/R_C$ is known as the load line. The dc bias point, or quiescent point, $Q$ will be at the intersection of the load line and the $i_C-v_{CE}$ curve corresponding to the base current $I_B$. The coordinates of point $Q$ give the dc collector current $I_C$ and the dc collector-to-emitter voltage $V_{CE}$. Observe that for amplifier operation, $Q$ should be in the active region and furthermore should be located so as to allow for a reasonable signal swing as the input signal $v_i$ is applied. This will become clearer shortly.

The situation when $v_i$ is applied is illustrated in Fig. 5.30. Consider first Fig. 5.30(a), which shows a signal $v_i$ having a triangular waveform being superimposed on the dc voltage $V_{CC}$. Corresponding to each instantaneous value of $V_{BB} = v(t)$, one can draw a straight line with slope $-1/R_C$. Such an “instantaneous load line” intersects the $i_B-v_{BE}$ curve at a point whose coordinates give the total instantaneous values of $i_B$ and $v_{BE}$ corresponding to the particular value of $V_{BB} = v(t)$. As an example, Fig. 5.30(a) shows the straight lines corresponding to $v_i = 0$, $v_i$ at its positive peak, and $v_i$ at its negative peak. Now, if the amplitude of $v_i$ is sufficiently small so that the instantaneous operating point is confined to an almost-linear segment of the $i_B-v_{BE}$ curve, then the resulting signals $i_b$ and $v_{be}$ will be triangular in waveform, as indicated in the figure. This, of course, is the small-signal approximation. In summary,

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*The term load line is also employed for the straight line in Fig. 5.28.*
FIGURE 5.30  Graphical determination of the signal components $v_{be}$, $i_b$, $i_c$, and $v_{ce}$ when a signal component $v_i$ is superimposed on the dc voltage $V_{BB}$ (see Fig. 5.27).
CHAPTER 5  BIPOLAR JUNCTION TRANSISTORS (BJTs)

the graphical construction in Fig. 5.30(a) can be used to determine the total instantaneous value of \( i_B \) corresponding to each value of \( v_i \).

Next, we move to the \( i_C – v_{CE} \) characteristics of Fig. 5.30(b). The operating point will move along the load line of slope \(-1/R_C\) as \( i_B \) goes through the instantaneous values determined from Fig. 5.30(a). For example, when \( v_i \) is at its positive peak, \( i_B = i_B^2 \) (from Fig. 5.30(a)), and the instantaneous operating point in the \( i_C – v_{CE} \) plane will be at the intersection of the load line and the curve corresponding to \( i_B = i_B^2 \). In this way, one can determine the waveforms of \( i_C \) and \( v_{CE} \) and hence of the signal components \( i_c \) and \( v_{ce} \), as indicated in Fig. 5.30(b).

Effects of Bias-Point Location on Allowable Signal Swing

The location of the dc bias point in the \( i_C – v_{CE} \) plane significantly affects the maximum allowable signal swing at the collector. Refer to Fig. 5.30(b) and observe that the positive peaks of \( v_{ce} \) cannot go beyond \( V_{CC} \), otherwise the transistor enters the cutoff region. Similarly, the negative peaks of \( v_{ce} \) cannot extend below a few tenths of a volt (usually, 0.3 V), otherwise the transistor enters the saturation region. The location of the bias point in Fig. 5.30(b) allows for an approximately equal swing in each direction.

Next consider Fig. 5.31. Here we show load lines corresponding to two values of \( R_C \). Line A corresponds to a low value of \( R_C \) and results in the operating point \( Q_A \), where the value of \( V_{CE} \) is very close to \( V_{CC} \). Thus the positive swing of \( v_{ce} \) will be severely limited; in this situation, it is said that there isn’t sufficient “head room.” On the other hand, line B, which corresponds to a large \( R_C \), results in the bias point \( Q_B \), whose \( V_{CE} \) is too low. Thus for line B, although there is ample room for the positive excursion of \( v_{ce} \) (there is a lot of head room), the negative signal swing is severely limited by the proximity to the saturation region (there is not sufficient “leg room”). A compromise between these two situations is obviously called for.

**FIGURE 5.31** Effect of bias-point location on allowable signal swing: Load-line A results in bias point \( Q_A \) with a corresponding \( V_{CE} \) which is too close to \( V_{CC} \) and thus limits the positive swing of \( v_{ce} \). At the other extreme, load-line B results in an operating point too close to the saturation region, thus limiting the negative swing of \( v_{ce} \).
5.3 THE BJT AS AN AMPLIFIER AND AS A SWITCH

5.3.4 Operation as a Switch
To operate the BJT as a switch, we utilize the cutoff and the saturation modes of operation. To illustrate, consider once more the common-emitter circuit shown in Fig. 5.32 as the input \(v_i\) is varied. For \(v_i\) less than about 0.5 V, the transistor will be cutoff; thus \(i_B = 0\), \(i_C = 0\), and \(v_C = V_{CC}\). In this state, node C is disconnected from ground; the switch is in the open position.

To turn the transistor on, we have to increase \(v_i\) above 0.5 V. In fact, for appreciable currents to flow, \(v_{BE} \approx 0.7\) V and \(v_i \approx 0.7\) V. The base current will be

\[
i_B = \frac{v_i - V_E}{R_B}
\]

(Eq. 5.60)

and the collector current will be

\[
i_C = \beta i_B
\]

(Eq. 5.61)

which applies only when the device is in the active mode. This will be the case as long as the CBJ is not forward biased, that is, as long as \(v_C > v_B - 0.4\) V, where \(v_C\) is given by

\[
v_C = V_{CC} - R_C i_C
\]

(Eq. 5.62)

Obviously, as \(v_i\) is increased, \(i_B\) will increase (Eq. 5.60), \(i_C\) will correspondingly increase (Eq. 5.61), and \(v_C\) will decrease (Eq. 5.62). Eventually, \(v_i\) will become lower than \(v_B\) by 0.4 V, at which point the transistor leaves the active region and enters the saturation region. This

EXERCISE

5.20 Consider the circuit of Fig. 5.27 with \(V_{BB} = 1.7\) V, \(R_B = 100\) kΩ, \(V_{CC} = 10\) V, and \(R_C = 5\) kΩ. Let the transistor \(\beta = 100\). The input signal \(v_i\) is a triangular wave of 0.4 V peak-to-peak. Refer to Fig. 5.30, and use the geometry of the graphical construction shown there to answer the following questions: (a) If \(V_{BE} = 0.7\) V, find \(I_B\). (b) Assuming operation on a straight line segment of the exponential \(i_B-v_{BE}\) curve, find \(I_C\) and \(V_{CE}\). (c) Find the inverse of its slope and compute its value. (d) What is the voltage gain of this amplifier?

Ans. (a) 10 \(\mu\)A; (b) 2.5 kΩ; (c) 4 \(\mu\)A; 10 mV; (d) 1 mA; 5 V; (e) 0.4 mA; 2 V; (f) -5 V/V
edge-of-saturation (EOS) point is defined by

$$I_{C(EOS)} = \frac{V_{CE} - 0.3}{R_C}$$

(5.63)

where we have assumed that $V_{BE}$ is approximately 0.7 V, and

$$I_{B(EOS)} = \frac{I_{C(EOS)}}{\beta}$$

(5.64)

The corresponding value of $V_B$ required to drive the transistor to the edge-of-saturation can be found from

$$V_{B(EOS)} = I_{B(EOS)}R_A + V_{BE}$$

(5.65)

Increasing $V_B$ above $V_{B(EOS)}$ increases the base current, which drives the transistor deeper into saturation. The collector-to-emitter voltage, however, decreases only slightly. As a reasonable approximation, we shall usually assume that for a saturated transistor, $V_{CE(sat)} \approx 0.2$ V.

The collector current then remains nearly constant at $I_{C(sat)}$

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C}$$

(5.66)

Forcing more current in the base has very little effect on $I_{C(sat)}$ and $V_{CE(sat)}$. In this state the switch is closed, with a low closure resistance $R_{CE(sat)}$ and a small offset voltage $V_{CE(off)}$ (see Fig. 5.24c).

Finally, recall that in saturation one can force the transistor to operate at any desired $\beta$ below the normal value; that is, the ratio of the collector current $I_{C(sat)}$ to the base current can be set at will and is therefore called the forced $\beta$.

$$\beta_{forced} = \frac{I_{C(sat)}}{I_B}$$

(5.67)

Also recall that the ratio of $I_B$ to $I_{B(EOS)}$ is known as the overdrive factor.

**EXAMPLE 5.3**

The transistor in Fig. 5.33 is specified to have $\beta$ in the range of 50 to 150. Find the value of $R_B$ that results in saturation with an overdrive factor of at least 10.

**Solution**

When the transistor is saturated, the collector voltage will be

$$V_C = V_{CE(sat)} \approx 0.2 \text{ V}$$
Thus the collector current is given by

\[ I_{\text{C, SAT}} = \frac{10 - 0.2}{1} = 9.8 \text{ mA} \]

To saturate the transistor with the lowest \( \beta \), we need to provide a base current of at least

\[ I_{\text{B(DSsat)}} = \frac{I_{\text{C, SAT}}}{\beta_{\text{min}}} = \frac{9.8}{50} = 0.196 \text{ mA} \]

For an overdrive factor of 10, the base current should be

\[ I_B = 10 \times 0.196 = 1.96 \text{ mA} \]

Thus we require a value of \( R_B \) such that

\[ \frac{5 - 0.7}{R_B} = 1.96 \]

\[ R_B = \frac{3.3}{1.94} = 2.2 \text{ k}\Omega \]

**EXERCISE**

5.21 Consider the circuit in Fig. 5.32 for the case \( V_{CC} = +5 \text{ V}, V_I = +5 \text{ V}, R_B = R_C = 1 \text{ k}\Omega, \) and \( \beta = 100. \)

Calculate the base current, the collector current, and the collector voltage. If the transistor is saturated, find \( \beta_{\text{forced}}. \) What should \( R_B \) be raised to bring the transistor to the edge of saturation?

**Ans.** 4.3 mA; 4.8 mA; 0.2 V; 1.1; 91.5 k\Omega

**5.4 BJT CIRCUITS AT DC**

We are now ready to consider the analysis of BJT circuits to which only dc voltages are applied. In the following examples we will use the simple model in which, \( V_{BE} \) of a conducting transistor is 0.7 V and \( V_{CE} \) of a saturated transistor is 0.2 V, and we will neglect the Early effect. Better models can, of course, be used to obtain more accurate results. Thus, however, is usually achieved at the expense of speed of analysis, and more importantly, it could impede the circuit designer’s ability to gain insight regarding circuit behavior. Accurate results using elaborate models can be obtained using circuit simulation with SPICE, as we shall see in Section 5.11. This is almost always done in the final stages of a design and certainly before circuit fabrication. Computer simulation, however, is not a substitute for quick pencil-and-paper circuit analysis, an essential ability that aspiring circuit designers must muster. The following series of examples is a step in that direction.

As will be seen, in analyzing a circuit the first question that one must answer is: In which mode is the transistor operating? In some cases, the answer will be obvious. In many cases, however, it will not. Needless to say, as the reader gains practice and experience in transistor circuit analysis and design, the answer will be obvious in a much larger proportion of problems. The answer, however, can always be determined by utilizing the following procedure:

Assume that the transistor is operating in the active mode, and proceed to determine the various voltages and currents. Then check for consistency of the results with the assumption of active-mode operation; that is, is \( V_{BE} \) of an npn transistor greater than \(-0.4 \text{ V}\) (or \( V_{CE} \) of a pnp transistor lower than \(0.4 \text{ V}\))? If the answer is yes, then our task is complete. If the answer
is no, assume saturation-mode operation, and proceed to determine currents and voltages and to check for consistency of the results with the assumption of saturation-mode operation. Here the test is usually to compute the ratio $I_C/I_E$ and to verify that it is lower than the transistor $\beta$, i.e., $I_C/I_E < \beta$. Since $\beta$ for a given transistor varies over a wide range, one should use the lowest specified $\beta$ for this test. Finally, note that the order of these two assumptions can be reversed.

**EXAMPLE 5.4**

Consider the circuit shown in Fig. 5.34(a), which is redrawn in Fig. 5.34(b) to remind the reader of the convention employed throughout this book for indicating connections to dc sources. We wish to analyze this circuit to determine all node voltages and branch currents. We will assume that $\beta$ is specified to be 100.

**FIGURE 5.34** Analysis of the circuit for Example 5.4: (a) circuit; (b) circuit redrawn to remind the reader of the convention used in this book to show connections to the power supply; (c) analysis with the steps numbered.
Solution
Glancing at the circuit in Fig. 5.34(a), we note that the base is connected to +4 V and the emitter is connected to ground through a resistance $R_E$. It therefore is safe to conclude that the base–emitter junction will be forward biased. Assuming that this is the case and assuming that $V_{BE}$ is approximately 0.7 V, it follows that the emitter voltage will be

$$V_E = 4 - V_{BE} \approx 4 - 0.7 = 3.3 \text{ V}$$

We are now in an opportune position; we know the voltages at the two ends of $R_E$ and thus can determine the current $I_E$ through it,

$$I_E = \frac{V_E - 0}{R_E} = \frac{3.3}{3.3} = 1 \text{ mA}$$

Since the collector is connected through $R_C$ to the +10-V power supply, it appears possible that the collector voltage will be higher than the base voltage, which is essential for active-mode operation. Assuming that this is the case, we can evaluate the collector current from

$$I_C = \alpha I_E$$

The value of $\alpha$ is obtained from

$$\alpha = \frac{\beta}{\beta + 1} = \frac{100}{101} \approx 0.99$$

Thus $I_C$ will be given by

$$I_C = 0.99 \times 1 = 0.99 \text{ mA}$$

We are now in a position to use Ohm’s law to determine the collector voltage $V_C$,

$$V_C = 10 - I_C R_C = 10 - 0.99 \times 4.7 = +5.3 \text{ V}$$

Since the base is at +4 V, the collector–base junction is reverse biased by 1.3 V, and the transistor is indeed in the active mode as assumed.

It remains only to determine the base current $I_B$ as follows:

$$I_B = \frac{I_E}{\beta + 1} = \frac{1}{101} \approx 0.01 \text{ mA}$$

Before leaving this example we wish to emphasize strongly the value of carrying out the analysis directly on the circuit diagram. Only in this way will one be able to analyze complex circuits in a reasonable length of time. Figure 5.34(c) illustrates the above analysis on the circuit diagram, with the order of the analysis steps indicated by the circled numbers.

EXAMPLE 5.5
We wish to analyze the circuit of Fig. 5.35(a) to determine the voltages at all nodes and the currents through all branches. Note that this circuit is identical to that of Fig. 5.34 except that the voltage at the base is now +6 V. Assume that the transistor $\beta$ is specified to be at least 50.
Solution

Assuming active-mode operation, we have

\[ V_E = +6 - V_{BE} = 6 - 0.7 = 5.3 \text{ V} \]
\[ I_E = \frac{5.3}{3.3} = 1.6 \text{ mA} \]
\[ V_C = +10 - 4.7 \times 1.6 \text{ mA} = 10 - 7.52 = 2.48 \text{ V} \]

The details of the analysis performed above are illustrated in Fig. 5.35(b).
Since the collector voltage calculated appears to be less than the base voltage by 3.52 V, it follows that our original assumption of active-mode operation is incorrect. In fact, the transistor has to be in the saturation mode. Assuming this to be the case, we have

\[ V_C = +6 - 0.7 = +5.3 \text{ V} \]
\[ I_E = \frac{V_C}{3.3} = \frac{5.3}{3.3} = 1.6 \text{ mA} \]
\[ V_C = V_E + V_{CE, sat} = +5.3 + 0.2 = +5.5 \text{ V} \]
\[ I_C = \frac{10 - 5.5}{4.7} = 0.96 \text{ mA} \]
\[ I_B = I_E - I_C = 1.6 - 0.96 = 0.64 \text{ mA} \]

Thus the transistor is operating at a forced \( \beta \) of \( \beta_{\text{forced}} = \frac{I_C}{I_E} = 0.96 \approx 1.5 \).

Since \( \beta_{\text{forced}} \) is less than the minimum specified value of \( \beta \), the transistor is indeed saturated. We should emphasize here that in testing for saturation the minimum value of \( \beta \) should be used. By the same token, if we are designing a circuit in which a transistor is to be saturated, the design should be based on the minimum specified \( \beta \). Obviously, if a transistor with this minimum \( \beta \) is saturated, then transistors with higher values of \( \beta \) will also be saturated. The details of the analysis are shown in Fig. 5.35(c), where the order of the steps used is indicated by the circled numbers.

**EXAMPLE 5.6**

We wish to analyze the circuit in Fig. 5.36(a) to determine the voltages at all nodes and the currents through all branches. Note that this circuit is identical to that considered in Examples 5.4 and 5.5 except that now the base voltage is zero.

\[ V_C = +6 \text{ V} \]
\[ I_E = \frac{10}{4.7} = 2.13 \text{ mA} \]
\[ I_C = \frac{3.3}{3.3} = 0 \text{ mA} \]
\[ I_B = 0 \text{ mA} \]

**FIGURE 5.36** Example 5.6: (a) circuit; (b) analysis with the order of the analysis steps indicated by circled numbers.
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Solution

Since the base is at zero volts, the emitter–base junction cannot conduct and the emitter current is zero. Also, the collector–base junction cannot conduct since the n-type collector is connected through \( R_C \) to the positive power supply while the p-type base is at ground. It follows that the collector current will be zero. The base current will also have to be zero, and the transistor is in the cutoff mode of operation.

The emitter voltage will obviously be zero, while the collector voltage will be equal to +10 V, since the voltage drop across \( R_C \) is zero. Figure 5.36(b) shows the analysis details.

EXERCISES

D5.22 For the circuit in Fig. 5.34(a), find the highest voltage to which the base can be raised while the transistor remains in the active mode. Assume \( \alpha \approx 1 \).

Ans. +4.7 V

D5.23 Redesign the circuit of Fig. 5.35(a) (i.e., find new values for \( R_E \) and \( R_C \)) to establish a collector current of 0.5 mA and a reverse-bias voltage on the collector–base junction of 2 V. Assume \( \alpha \approx 1 \).

Ans. \( R_E = 6.6 \, \text{k}\Omega; \quad R_C = 8 \, \text{k}\Omega \)

D5.24 For the circuit in Fig. 5.35(a), find the value to which the base voltage should be changed to so that the transistor operates in saturation with a forced \( \beta \) of 5.

Ans. +5.18 V
Solution

The base of this pnp transistor is grounded, while the emitter is connected to a positive supply \( V^+ = +10 \text{ V} \) through \( R_E \). It follows that the emitter–base junction will be forward biased with \( V_E = V_{EB} = 0.7 \text{ V} \).

Thus the emitter current will be given by

\[
I_E = \frac{V^+ - V_E}{R_E} = \frac{10 - 0.7}{2} = 4.65 \text{ mA}
\]

Since the collector is connected to a negative supply (more negative than the base voltage) through \( R_C \), it is possible that this transistor is operating in the active mode. Assuming this to be the case, we obtain

\[
I_C = \alpha I_E
\]

Since no value for \( \beta \) has been given, we shall assume \( \beta = 100 \), which results in \( \alpha = 0.99 \). Since large variations in \( \beta \) result in small differences in \( \alpha \), this assumption will not be critical as far as determining the value of \( I_C \) is concerned. Thus,

\[
I_C = 0.99 \times 4.65 = 4.6 \text{ mA}
\]

The collector voltage will be

\[
V_C = V^- + I_C R_C = -10 + 4.6 \times 1 = -5.4 \text{ V}
\]

Thus the collector–base junction is reverse biased by 5.4 V, and the transistor is indeed in the active mode, which supports our original assumption.

It remains only to calculate the base current,

\[
I_B = \frac{I_E}{\beta + 1} = \frac{4.65}{100} = 0.05 \text{ mA}
\]

Obviously, the value of \( \beta \) critically affects the base current. Note, however, that in this circuit the value of \( \beta \) will have no effect on the mode of operation of the transistor. Since \( \beta \) is generally an ill-specified parameter, this circuit represents a good design. As a rule, one should strive to design the circuit such that its performance is as insensitive to the value of \( \beta \) as possible. The analysis details are illustrated in Fig. 5.37(b).

EXERCISES

D5.25 For the circuit in Fig. 5.37(a), find the largest value to which \( R_C \) can be raised while the transistor remains in the active mode.

Ans. 2.26 k\( \Omega \)

D5.26 Redesign the circuit of Fig. 5.37(a) (i.e., find new values for \( R_E \) and \( R_C \)) to establish a collector current of 1 mA and a reverse bias on the collector–base junction of 4 V. Assume \( \alpha = 1 \).

Ans. \( R_E = 9.3 \text{ k}\Omega \); \( R_C = 6 \text{ k}\Omega \)
EXAMPLE 5.8

We want to analyze the circuit in Fig. 5.38(a) to determine the voltages at all nodes and the currents in all branches. Assume $\beta = 100$.

Solution

The base–emitter junction is clearly forward biased. Thus,

$$I_B = \frac{+5 - V_{BE}}{R_E} = \frac{5 - 0.7}{100} = 0.043 \text{ mA}$$

Assume that the transistor is operating in the active mode. We now can write

$$I_C = \beta I_B = 100 \times 0.043 = 4.3 \text{ mA}$$

The collector voltage can now be determined as

$$V_C = 10 - 2 \times 4.3 = +1.4 \text{ V}$$

Since the base voltage $V_B$ is

$$V_B = V_{BE} = +0.7 \text{ V}$$

it follows that the collector–base junction is reverse-biased by 0.7 V and the transistor is indeed in the active mode. The emitter current will be given by

$$I_E = (\beta + 1)I_B = 101 \times 0.043 = 4.343 \text{ mA}$$

We note from this example that the collector and emitter currents depend critically on the value of $\beta$. In fact, if $\beta$ were 10% higher, the transistor would leave the active mode and enter saturation. Therefore this clearly is a bad design. The analysis details are illustrated in Fig. 5.38(b).
EXAMPLE 5.9

We want to analyze the circuit of Fig. 5.39 to determine the voltages at all nodes and the currents through all branches. The minimum value of $\beta$ is specified to be 30.

Solution

A quick glance at this circuit reveals that the transistor will be either active or saturated. Assuming active-mode operation and neglecting the base current, we see that the base voltage will be approximately zero volts, the emitter voltage will be approximately $+0.7 \, \text{V}$, and the emitter current will be approximately $4.3 \, \text{mA}$. Since the maximum current that the collector can support while the transistor remains in the active mode is approximately $0.5 \, \text{mA}$, it follows that the transistor is definitely saturated.

Assuming that the transistor is saturated and denoting the voltage at the base by $V_B$ (refer to Fig. 5.39b), it follows that:

\[ V_E = V_B + V_{EB} \approx V_B + 0.7 \]
\[ V_C = V_B - V_{CE} \approx V_B + 0.7 - 0.2 = V_B + 0.5 \]
Using the relationship \( I_E = I_B + I_C \), we obtain which results in 

Substituting in the equations above, we obtain.

It is clear that the transistor is saturated, since the value of forced \( \beta \) is which is much smaller than the specified minimum \( \beta \).

**EXAMPLE 5.10**

We want to analyze the circuit of Fig. 5.40(a) to determine the voltages at all nodes and the currents through all branches. Assume \( \beta = 100 \).

**Solution**

The first step in the analysis consists of simplifying the base circuit using Thévenin’s theorem.

The result is shown in Fig. 5.40(b), where

\[
V_{BB} = +15 - \frac{R_{BB}}{R_{BB} + R_E} = +15 - \frac{50}{100 + 50} = +5 \text{ V}
\]

\[
R_{BB} = (R_B || R_E) = (100 || 50) = 33.3 \text{ kΩ}
\]

To evaluate the base or the emitter current, we have to write a loop equation around the loop marked L in Fig. 5.40(b). Note, though, that the current through \( R_{BB} \) is different from the current through \( R_E \). The loop equation will be

\[
V_{BB} = I_B R_{BB} + V_{BE} + I_E R_E
\]
Substituting for $I_B$ by

$$I_B = \frac{I_E}{\beta + 1}$$

and rearranging the equation gives

$$I_E = \frac{V_{BE} - V_{CE}}{R_E + (R_E/\beta + 1)}$$

For the numerical values given we have

$$I_E = \frac{5 - 0.7}{3 + \left(\frac{33.3}{101}\right)} = 1.29 \text{ mA}$$

The base current will be

$$I_B = \frac{1.29}{101} = 0.0128 \text{ mA}$$
The base voltage is given by
\[ V_b = V_{bb} + I_b R_b \]
\[ = 0.7 + 1.29 \times 3 = 4.57 \text{ V} \]
Assume active-mode operation. We can evaluate the collector current as
\[ I_C = a I_B = 0.99 \times 1.29 = 1.28 \text{ mA} \]
The collector voltage can now be evaluated as
\[ V_C = V_{bb} - I_C R_C = 15 - 1.28 \times 5 = 8.6 \text{ V} \]
It follows that the collector is higher in potential than the base by 4.03 V, which means that the transistor is in the active mode, as had been assumed. The results of the analysis are given in Fig. 5.40(c).

**EXAMPLE 5.11**  
We wish to analyze the circuit in Fig. 5.41(a) to determine the voltages at all nodes and the currents through all branches.

**Solution**  
We first recognize that part of this circuit is identical to the circuit we analyzed in Example 5.10—namely, the circuit of Fig. 5.40(a). The difference, of course, is that in the new circuit we have an additional transistor \( Q_2 \) together with its associated resistors \( R_{E2} \) and \( R_{C2} \). Assume that \( Q_1 \) is still in the active mode. The following values will be identical to those obtained in the previous example:
\[ V_{bb} = 4.57 \text{ V} \]
\[ I_{B1} = 1.29 \text{ mA} \]
\[ I_{E1} = 0.0128 \text{ mA} \]
\[ I_{C1} = 1.28 \text{ mA} \]
However, the collector voltage will be different than previously calculated since part of the collector current \( I_{C1} \) will flow in the base lead of \( Q_2 (I_{B2}) \). As a first approximation we may assume that \( I_{B2} \) is much smaller than \( I_{C1} \); that is, we may assume that the current through \( R_{C1} \) is almost equal to \( I_{C1} \). This will enable us to calculate \( V_{C1} \):
\[ V_{C1} = V_{bb} - I_{C1} R_{C1} \]
\[ = 15 - 1.28 \times 5 = 8.6 \text{ V} \]
Thus \( Q_1 \) is in the active mode, as had been assumed.

**EXERCISE 5.28**  
If the transistor in the circuit of Fig. 5.40(a) is replaced with another having half the value of \( \beta \) (i.e., \( \beta = 50 \)), find the new value of \( I_C \), and express the change in \( I_C \) as a percentage.

**Ans.** \( I_C = 1.15 \text{ mA}; -10\% \)
As far as $Q_2$ is concerned, we note that its emitter is connected to +15 V through $R_{E2}$. It is therefore safe to assume that the emitter–base junction of $Q_2$ will be forward biased. Thus the emitter of $Q_2$ will be at a voltage $V_{E2}$ given by

$$V_{E2} = V_{E1} + V_{BE} = 8.6 + 0.7 = +9.3 \text{ V}$$

The emitter current of $Q_2$ may now be calculated as

$$I_{E2} = \frac{15 - V_{E2}}{R_{E2}} = \frac{15 - 9.3}{2} = 2.85 \text{ mA}$$
Since the collector of \( Q_2 \) is returned to ground via \( R_{C2} \), it is possible that \( Q_2 \) is operating in the active mode. Assume this to be the case. We now find \( I_{C2} \) as

\[
I_{C2} = \alpha_2 I_{E2} = 0.99 \times 2.85 = 2.82 \text{ mA} \quad \text{(assuming } \beta_2 = 100) \]

The collector voltage of \( Q_2 \) will be

\[
V_{C2} = I_{C2}R_{C2} = 2.82 \times 2.7 = 7.62 \text{ V} \]

which is lower than \( V_{CB} \) by 0.98 V. Thus \( Q_2 \) is in the active mode, as assumed.

It is important at this stage to find the magnitude of the error incurred in our calculations by the assumption that \( I_{B2} \) is negligible. The value of \( I_{B2} \) is given by

\[
I_{B2} = \frac{I_{E2}}{\beta_2 + 1} = \frac{2.85}{101} = 0.028 \text{ mA} \]

which is indeed much smaller than \( I_{C1} \) (1.28 mA). If desired, we can obtain more accurate results by iterating one more time, assuming \( I_{B2} \) to be 0.028 mA. The new values will be

\[
I_{C2} = \frac{I_{E2}}{\beta_2 + 1} = \frac{2.85}{101} = 0.028 \text{ mA} \]

Current in \( R_{C1} \) is \( I_{C1} - I_{C2} = 1.28 - 0.028 = 1.252 \text{ mA} \)

\[
V_{C1} = 15 - 5 \times 1.252 = 8.74 \text{ V} \\
V_{E2} = 8.74 + 0.7 = 9.44 \text{ V} \\
I_{E2} = \frac{15 - 9.44}{2} = 2.78 \text{ mA} \\
I_{C2} = 0.99 \times 2.78 = 2.75 \text{ mA} \\
V_{C2} = 2.75 \times 2.7 = 7.43 \text{ V} \\
I_{E2} = \frac{2.78}{101} = 0.0275 \text{ mA} \\
I_{C2} = \frac{2.78}{101} = 0.0275 \text{ mA} \\
V_{C2} = 2.75 \times 2.7 = 7.43 \text{ V} \\
I_{E2} = \frac{2.78}{101} = 0.0275 \text{ mA} \\
V_{C2} = 2.75 \times 2.7 = 7.43 \text{ V} \\
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V_{C2} = 2.75 \times 2.7 = 7.43 \text{ V} \\
I_{E2} = \frac{2.78}{101} = 0.0275 \text{ mA} \\
V_{C2} = 2.75 \times 2.7 = 7.43 \text{ V} \\
I_{E2} = \frac{2.78}{101} = 0.0275 \text{ mA} \\
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I_{E2} = \frac{2.78}{101} = 0.0275 \text{ mA} \\
V_{C2} = 2.75 \times 2.7 = 7.43 \text{ V} \\
I_{E2} = \frac{2.78}{101} = 0.0275 \text{ mA} \\
V_{C2} = 2.75 \times 2.7 = 7.43 \text{ V} \\
I_{E2} = \frac{2.78}{101} = 0.0275 \text{ mA} \\
V_{C2} = 2.75 \times 2.7 = 7.43 \text{ V} \\
I_{E2} = \frac{2.78}{101} = 0.0275 \text{ mA} \\
V_{C2} = 2.75 \times 2.7 = 7.43 \text{ V} \\
I_{E2} = \frac{2.78}{101} = 0.0275 \text{ mA} \\
V_{C2} = 2.75 \times 2.7 = 7.43 \text{ V} \\
I_{E2} = \frac{2.78}{101} = 0.0275 \text{ mA} \\
V_{C2} = 2.75 \times 2.7 = 7.43 \text{ V} \\n
Note that the new value of \( I_{E2} \) is very close to the value used in our iteration, and no further iterations are warranted. The final results are indicated in Fig. 5.41(b).

The reader justifiably might be wondering about the necessity for using an iterative scheme in solving a linear (or linearized) problem. Indeed, we can obtain the exact solution (if we can call anything we are doing with a first-order model exact!) by writing appropriate equations. The reader is encouraged to find this solution and then compare the results with those obtained above.

It is important to emphasize, however, that in most such problems it is quite sufficient to obtain an approximate solution, provided that we can obtain it quickly and, of course, correctly.

In the above examples, we frequently used a precise value of \( \alpha \) to calculate the collector current. Since \( \alpha = 1 \), the error in such calculations will be very small if one assumes \( \alpha = 1 \) and \( I_C = I_E \). Therefore, except in calculations that depend critically on the value of \( \alpha \) (e.g., the calculation of base current), one usually assumes \( \alpha = 1 \).

**EXERCISES**

5.29 For the circuit in Fig. 5.41, find the total current drawn from the power supply. Hence find the power dissipated in the circuit.

*Ans.* 4.135 mA; 62 mW
EXAMPLE 5.12

We desire to evaluate the voltages at all nodes and the currents through all branches in the circuit of Fig. 5.42(a). Assume $\beta = 100$.

Solution

By examining the circuit we conclude that the two transistors $Q_1$ and $Q_2$ cannot be simultaneously conducting. Thus if $Q_1$ is on, $Q_2$ will be off, and vice versa. Assume that $Q_2$ is on. It
follows that current will flow from ground through the 1-kΩ load resistor into the emitter of \(Q_2\). Thus the base of \(Q_2\) will be at a negative voltage, and base current will be flowing out of the base through the 10-kΩ resistor and into the +5-V supply. This is impossible, since if the base is negative, current in the 10-kΩ resistor will have to flow into the base. Thus we conclude that our original assumption—that \(Q_2\) is on—is incorrect. It follows that \(Q_2\) will be off and \(Q_1\) will be on.

The question now is whether \(Q_1\) is active or saturated. The answer in this case is obvious. Since the base is fed with a +5-V supply and since base current flows into the base of \(Q_1\), it follows that the base of \(Q_1\) will be at a voltage lower than +5 V. Thus the collector–base junction of \(Q_1\) is reverse biased and \(Q_1\) is in the active mode. It remains only to determine the currents and voltages using techniques already described in detail. The results are given in Fig. 5.42(b).

### 5.5 BIASING IN BJT AMPLIFIER CIRCUITS

The biasing problem is that of establishing a constant dc current in the collector of the BJT. This current has to be calculable, predictable, and insensitive to variations in temperature and to the large variations in the value of \(\beta\) encountered among transistors of the same type. Another important consideration in bias design is locating the dc bias point in the \(i_C–v_{CE}\) plane to allow for maximum output signal swing (see the discussion in Section 5.3.3). In this section, we shall deal with various approaches to solving the bias problem in transistor circuits designed with discrete devices. Bias methods for integrated-circuit design are presented in Chapter 6.

Before presenting the “good” biasing schemes, we should point out why two obvious arrangements are not good. First, attempting to bias the BJT by fixing the voltage \(V_{BE}\) by, for instance, using a voltage divider across the power supply \(V_{CC}\), as shown in Fig. 5.43(a), is not a viable approach. The very sharp exponential relationship \(i_C–v_{BE}\) means that any small and inevitable differences in \(V_{BE}\) from the desired value will result in large differences in \(I_C\) and in \(V_{CE}\). Second, biasing the BJT by establishing a constant current in the base, as shown in Fig. 5.43(b), where \(I_B = (V_{CC} - 0.7)/R_B\), is also not a recommended approach. Here the typically large variations in the value of \(\beta\) among units of the same device type will result in correspondingly large variations in \(I_B\) and hence in \(V_{CE}\).

#### 5.5.1 Classical Discrete-Circuit Bias Arrangement

Figure 5.44(a) shows the arrangement most commonly used for biasing a discrete-circuit transistor amplifier if only a single power supply is available. The technique consists of supplying the base of the transistor with a fraction of the supply voltage \(V_{CC}\) through the voltage divider \(R_B, R_E\). In addition, a resistor \(R_E\) is connected to the emitter.

**EXERCISE**

5.31 Solve the problem in Example 5.12 with the voltage feeding the bases changed to +10 V. Assume that \(\beta_{min} = 30\), and find \(V_{BE}, V_B, I_C1,\) and \(I_C2\).

**Ans.** +4.8 V; +5.5 V; 4.35 mA; 0
5.5 Biasing in BJT Amplifier Circuits

Figure 5.44(b) shows the same circuit with the voltage-divider network replaced by its Thévenin equivalent,

\[
V_{BB} = V_C \left( \frac{R_1}{R_1 + R_2} \right) \quad (5.68)
\]

\[
R_B = \frac{R_1 R_2}{R_1 + R_2} \quad (5.69)
\]

The current \(I_B\) can be determined by writing a Kirchhoff loop equation for the base–emitter–ground loop, labeled \(L\), and substituting \(I_B = I_E/(\beta + 1)\):

\[
I_E = \frac{V_{BB} - V_{BE}}{R_E + R_E/(\beta + 1)} \quad (5.70)
\]
To make $I_E$ insensitive to temperature and $\beta$ variation, we design the circuit to satisfy the following two constraints:

$$V_{BB} \gg V_{BE}$$  \hspace{1cm} (5.71)

$$R_L \approx \frac{R_B}{\beta + 1}$$  \hspace{1cm} (5.72)

Condition (5.71) ensures that small variations in $V_{BB}$ (≈0.7 V) will be swamped by the much larger $V_{BB}$. There is a limit, however, on how large $V_{BB}$ can be: For a given value of the supply voltage $V_{CC}$, the higher the value we use for $V_{BB}$, the lower will be the sum of voltages across $R_L$ and the collector–base junction ($V_{CB}$). On the other hand, we want the voltage across $R_L$ to be large in order to obtain high voltage gain and large signal swing (before transistor cutoff). We also want $V_{CB}$ (or $V_{CE}$) to be large to provide a large signal swing (before transistor saturation). Thus, as is the case in any design problem, we have a set of conflicting requirements, and the solution must be a compromise. As a rule of thumb, one designs for $V_{BB}$ about $\frac{1}{3}V_{CC}$, $V_{CE}$ (or $V_{CB}$) about $\frac{2}{3}V_{CC}$, and $I_E R_C$ about $\frac{1}{3}V_{CE}$.

Condition (5.72) makes $I_E$ insensitive to variations in $\beta$ and could be satisfied by selecting $R_B$ small. This in turn is achieved by using low values for $R_1$ and $R_2$. Lower values for $R_1$ and $R_2$, however, will mean a higher current drain from the power supply and normally will result in a lowering of the input resistance of the amplifier (if the input signal is coupled to the base), which is the trade-off involved in this part of the design problem. It should be noted that Condition (5.72) means that we want to make the base voltage independent of the value of $\beta$ and determined solely by the voltage divider. This will obviously be satisfied if the current in the divider is made much larger than the base current. Typically one selects $R_1$ and $R_2$ such that their current is in the range of $I_E$ to 0.1$I_E$.

Further insight regarding the mechanism by which the bias arrangement of Fig. 5.44(a) stabilizes the dc emitter (and hence collector) current is obtained by considering the feedback action provided by $R_E$. Consider that for some reason the emitter current increases. The voltage drop across $R_E$, and hence $V_E$ will increase correspondingly. Now, if the base voltage is determined primarily by the voltage divider $R_1$, $R_2$, which is the case if $R_B$ is small, it will remain constant, and the increase in $V_E$ will result in a corresponding decrease in $V_{CE}$. This in turn reduces the collector (and emitter) current, a change opposite to that originally assumed. Thus $R_E$ provides a negative feedback action that stabilizes the bias current. We shall study negative feedback formally in Chapter 9.

**EXAMPLE 5.13**

We wish to design the bias network of the amplifier in Fig. 5.44 to establish a current $I_E = 1$ mA using a power supply $V_{CC} = +12$ V. The transistor is specified to have a nominal $\beta$ value of 100.

**Solution**

We shall follow the rule of thumb mentioned above and allocate one-third of the supply voltage to the voltage drop across $R_1$ and another one-third to the voltage drop across $R_2$, leaving one-third

---

8 Bias design seeks to stabilize either $I_E$ or $I_C$ since $I_C = \alpha I_E$ and $\alpha$ varies very little. That is, a stable $I_E$ will result in an equally stable $I_C$, and vice versa.
for possible signal swing at the collector. Thus,

\[
V_b = +4 \text{ V} \\
V_C = 4 - V_{BE} = 3.3 \text{ V}
\]

and \( R_E \) is determined from

\[
R_E = \frac{V_C}{I_E} = 3.3 \text{ k}\Omega
\]

From the discussion above we select a voltage-divider current of \( 0.1I_E = 0.1 \times 1 = 0.1 \text{ mA} \). Neglecting the base current, we find

\[
R_1 + R_2 = \frac{12}{0.1} = 120 \text{ k}\Omega
\]

and

\[
\frac{R_1}{R_1 + R_2} V_{CC} = 4 \text{ V}
\]

Thus \( R_1 = 40 \text{ k}\Omega \) and \( R_2 = 80 \text{ k}\Omega \).

At this point, it is desirable to find a more accurate estimate for \( I_E \), taking into account the nonzero base current. Using Eq. (5.70),

\[
I_E = \frac{4 - 0.7}{3.3(\text{k}\Omega) + \frac{20(0.7)(\text{k}\Omega)}{101}} = 0.93 \text{ mA}
\]

This is quite a bit lower than the value we are aiming for of 1 mA. It is easy to see from the above equation that a simple way to restore \( I_E \) to its nominal value would be to reduce \( R_E \) from 3.3 k\Omega by the magnitude of the second term in the denominator (0.267 k\Omega). Thus a more suitable value for \( R_E \) in this case would be \( R_E = 3 \text{ k}\Omega \), which results in \( I_E = 1.01 \text{ mA} \approx 1 \text{ mA} \).

It should be noted that if we are willing to draw a higher current from the power supply and to accept a lower input resistance for the amplifier, then we may use a voltage-divider current equal, say, to \( I_E \) (i.e., 1 mA), resulting in \( R_1 = 8 \text{ k}\Omega \) and \( R_2 = 4 \text{ k}\Omega \). We shall refer to the circuit using these latter values as design 2, for which the actual value of \( I_E \) using the initial value of \( R_E \) of 3.3 k\Omega will be

\[
I_E = \frac{4 - 0.7}{3.3 + 0.027} = 0.99 \approx 1 \text{ mA}
\]

In this case, design 2, we need not change the value of \( R_E \).

Finally, the value of \( R_C \) can be determined from

\[
R_C = \frac{12 - V_C}{I_E}
\]

Substituting \( I_E = \alpha I_E = 0.99 \times 1 = 0.99 \text{ mA} \approx 1 \text{ mA} \) results, for both designs, in

\[
R_C = \frac{12 - 8}{1} = 4 \text{ k}\Omega
\]
5.5.2 A Two Power-Supply Version of the Classical Bias Arrangement

A somewhat simpler bias arrangement is possible if two power supplies are available, as shown in Fig. 5.45. Writing a loop equation for the loop labeled L gives

$$I_e = \frac{V_{EE} - V_{BE}}{R_e + R_f/\beta + 1}$$

(5.73)

This equation is identical to Eq. (5.70) except for $V_{EE}$ replacing $V_{BB}$. Thus the two constraints of Eqs. (5.71) and (5.72) apply here as well. Note that if the transistor is to be used with the base grounded (i.e., in the common-base configuration), then $R_f$ can be eliminated altogether. On the other hand, if the input signal is to be coupled to the base, then $R_f$ is needed. We shall study the various BJT amplifier configurations in Section 5.7.

EXERCISE

5.32 For design 1 in Example 5.13, calculate the expected range of $I_e$ if the transistor used has $\beta$ in the range of 50 to 150. Express the range of $I_e$ as a percentage of the nominal value ($I_e = 1$ mA) obtained for $\beta = 100$. Repeat for design 2.

Ans. For design 1: 0.94 mA to 1.04 mA a 10% range; for design 2: 0.984 mA to 0.995 mA, a 1.1% range.

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Ans. For design 1: 0.94 mA to 1.04 mA a 10% range; for design 2: 0.984 mA to 0.995 mA, a 1.1% range.

EXERCISE

D5.33 The bias arrangement of Fig. 5.45 is to be used for a common-base amplifier. Design the circuit to establish a dc emitter current of 1 mA and provide the highest possible voltage gain while allowing for a maximum signal swing at the collector of ±2 V. Use +10-V and −5-V power supplies.

Ans. $R_f = 0$; $R_e = 4.3$ k$\Omega$; $R_c = 8.4$ k$\Omega$
5.5 BIASING IN BJT AMPLIFIER CIRCUITS

5.5.3 Biasing Using a Collector-to-Base Feedback Resistor

Figure 5.46(a) shows a simple but effective alternative biasing arrangement suitable for common-emitter amplifiers. The circuit employs a resistor $R_B$ connected between the collector and the base. Resistor $R_B$ provides negative feedback, which helps to stabilize the bias point of the BJT. We shall study feedback formally in Chapter 9.

Analysis of the circuit is shown in Fig. 5.46(b), from which we can write

$$ V_{CC} = I_k R_C + I_k R_B + V_{BE} $$

Thus the emitter bias current is given by

$$ I_E = \frac{V_{CC} - V_{BE}}{R_C + R_B / (\beta + 1)} $$  \hspace{1cm} (5.74) $$

It is interesting to note that this equation is identical to Eq. (5.70), which governs the operation of the traditional bias circuit, except that $V_{CC}$ replaces $V_{BB}$ and $R_C$ replaces $R_E$. It follow that to obtain a value of $I_E$ that is insensitive to variation of $\beta$, we select $R_B / (\beta + 1) \ll R_C$.

Note, however, that the value of $R_B$ determines the allowable signal swing at the collector since

$$ V_{CB} = I_k R_B = I_k R_B / \beta + 1 $$  \hspace{1cm} (5.75) $$

EXERCISE

**D5.34** Design the circuit of Fig. 5.46 to obtain a dc emitter current of 1 mA and to ensure a ±2-V signal swing at the collector; that is, design for $V_{CC} = +2.4$ V. Let $V_{CC} = 10$ V and $\beta = 100$.

**Ans.** $R_B = 172$ k$\Omega$; $R_C = 7.6$ k$\Omega$. Note that if standard 5% resistor values are used (Appendix H) we select $R_B = 180$ k$\Omega$ and $R_C = 7.5$ k$\Omega$. This results in $I_E = 1.00$ mA and $V_C = +2.5$ V.
5.5.4 Biasing Using a Constant-Current Source

The BJT can be biased using a constant-current source $I$ as indicated in the circuit of Fig. 5.47(a). This circuit has the advantage that the emitter current is independent of the values of $\beta$ and $R_B$. Thus $R_B$ can be made large, enabling an increase in the input resistance at the base without adversely affecting bias stability. Further, current-source biasing leads to significant design simplification, as will become obvious in later sections and chapters.

A simple implementation of the constant-current source $I$ is shown in Fig. 4.47(b). The circuit utilizes a pair of matched transistors $Q_1$ and $Q_2$, with $Q_1$ connected as a diode by shorting its collector to its base. If we assume that $Q_1$ and $Q_2$ have high $\beta$ values, we can neglect their base currents. Thus the current through $Q_1$ will be approximately equal to $I_{REF}$,

$$I_{REF} = \frac{V_{CC} - (-V_{BE}) - V_{EE}}{R}$$

(5.76)

Now, since $Q_1$ and $Q_2$ have the same $V_{BE}$, their collector currents will be equal, resulting in

$$I = I_{REF} = \frac{V_{CC} + V_{EE} - V_{BE}}{R}$$

(5.77)

Neglecting the Early effect in $Q_2$, the collector current will remain constant at the value given by this equation as long as $Q_2$ remains in the active region. This can be guaranteed by keeping the voltage at the collector $V$ greater than that at the base ($-V_{BE} + V_{EE}$). The connection of $Q_1$ and $Q_2$ in Fig. 4.47(b) is known as a current mirror. We will study current mirrors in detail in Chapter 6.

**EXERCISE**

5.35 For the circuit in Fig. 5.47(a) with $V_{CC} = 10$ V, $I = 1$ mA, $\beta = 100$, $R_B = 100$ k$\Omega$, and $R_C = 7.5$ k$\Omega$, find the dc voltage at the base, the emitter, and the collector. For $V_{EE} = 10$ V, find the value of $R$ in the circuit of Fig. 5.47(b).

Ans. $-1$ V, $-1.7$ V, $+2.6$ V; 19.3 k$\Omega$
5.6 SMALL-SIGNAL OPERATION AND MODELS

Having learned how to bias the BJT to operate as an amplifier, we now take a closer look at the small-signal operation of the transistor. Toward that end, consider the conceptual circuit shown in Fig. 5.48(a). Here the base-emitter junction is forward biased by a dc voltage $V_{BE}$ (battery). The reverse bias of the collector-base junction is established by connecting the collector to another power supply of voltage $V_{CC}$ through a resistor $R_C$. The input signal to be amplified is represented by the voltage source $v_{be}$ that is superimposed on $V_{BE}$.

We consider first the dc bias conditions by setting the signal $v_{be}$ to zero. The circuit reduces to that in Fig. 5.48(b), and we can write the following relationships for the dc currents and voltages:

\[
\begin{align*}
I_C &= I_S e^{v_{be}/V_T} \\
I_E &= I_S / \alpha \\
I_B &= I_S / \beta \\
V_C &= V_{CE} = V_{CC} - I_C R_C
\end{align*}
\]

Obviously, for active-mode operation, $V_C$ should be greater than $(V_E - 0.4)$ by an amount that allows for a reasonable signal swing at the collector.

5.6.1 The Collector Current and the Transconductance

If a signal $v_{be}$ is applied as shown in Fig. 5.48(a), the total instantaneous base-emitter voltage $V_{BE}$ becomes

\[v_{BE} = V_{BE} + v_{be}\]

Correspondingly, the collector current becomes

\[
\begin{align*}
i_C &= I_S e^{v_{be}/V_T} = I_S e^{(V_{BE} + v_{be})/V_T} \\
&= I_S e^{V_{BE}/V_T} e^{v_{be}/V_T}
\end{align*}
\]

![FIGURE 5.48](a) Conceptual circuit to illustrate the operation of the transistor as an amplifier. (b) The circuit of (a) with the signal source $v_{be}$ eliminated for dc (bias) analysis.)
Use of Eq. (5.78) yields

$$i_C = I_C e^{v_{be}/V_T} \quad (5.82)$$

Now, if $v_{be} \ll V_T$, we may approximate Eq. (5.82) as

$$i_C = I_C \left(1 + \frac{v_{be}}{V_T}\right) \quad (5.83)$$

Here we have expanded the exponential in Eq. (5.82) in a series and retained only the first two terms. This approximation, which is valid only for $v_{be}$ less than approximately 10 mV, is referred to as the small-signal approximation. Under this approximation the total collector current is given by Eq. (5.83) and can be rewritten

$$i_C = I_C + \frac{dC_{be}}{V_T} v_{be} \quad (5.84)$$

Thus the collector current is composed of the dc bias value $I_C$ and a signal component $i_c$.

$$i_C = \frac{I_C v_{be}}{V_T} \quad (5.85)$$

This equation relates the signal current in the collector to the corresponding base–emitter signal voltage. It can be rewritten as

$$\frac{dC_{be}}{V_T} = g_m v_{be} \quad (5.86)$$

where $g_m$ is called the transconductance, and from Eq. (5.85), it is given by

$$g_m = \frac{I_C}{V_T} \quad (5.87)$$

We observe that the transconductance of the BJT is directly proportional to the collector bias current $I_C$. Thus to obtain a constant predictable value for $g_m$, we need a constant predictable $I_C$. Finally, we note that BJTs have relatively high transconductance (as compared to MOSFETs, which we studied in Chapter 4); for instance, at $I_C = 1$ mA, $g_m = 40$ mA/V.

A graphical interpretation for $g_m$ is given in Fig. 5.49, where it is shown that $g_m$ is equal to the slope of the $i_C$ vs. $v_{be}$ characteristic curve at $i_C = I_C$ (i.e., at the bias point $Q$). Thus,

$$g_m = \frac{\partial i_C}{\partial v_{be}} \bigg|_{i_C = I_C} \quad (5.88)$$

The small-signal approximation implies keeping the signal amplitude sufficiently small so that operation is restricted to an almost-linear segment of the $i_C$ vs. $v_{be}$ exponential curve. Increasing the signal amplitude will result in the collector current having components nonlinearly related to $v_{be}$. This, of course, is the same approximation we discussed in the context of the amplifier transfer curve in Section 5.3.

The analysis above suggests that for small signals ($v_{be} \ll V_T$), the transistor behaves as a voltage-controlled current source. The input port of this controlled source is between base and emitter, and the output port is between collector and emitter. The transconductance of the controlled source is $g_m$, and the output resistance is infinite. The latter ideal property is a result of our first-order model of transistor operation in which the collector voltage has no effect on the collector current in the active mode. As we have seen in Section 5.2, practical
BJTs have finite output resistance because of the Early effect. The effect of the output resistance on amplifier performance will be considered later.

**EXERCISE**

5.36 Use Eq. (5.88) to derive the expression for $g_m$ in Eq. (5.87).

### 5.6.2 The Base Current and the Input Resistance at the Base

To determine the resistance seen by $v_{be}$, we first evaluate the total base current $i_b$ using Eq. (5.84), as follows:

$$i_b = \frac{i_c}{\beta} - \frac{I_c}{\beta} + \frac{I_c}{\beta} \frac{v_{be}}{V_T}$$

Thus,

$$i_b = i_b + i_s$$

where $i_b$ is equal to $I_c/\beta$ and the signal component $i_s$ is given by

$$i_s = \frac{I_c}{\beta} \frac{v_{be}}{V_T}$$

where $V_T$ is the thermal voltage.
Substituting for $I_C/V_T$ by $g_m$ gives

$$i_b = \frac{g_m}{\beta} v_{be}$$  \hspace{1cm} (5.91)

The small-signal input resistance between base and emitter, looking into the base, is denoted by $r_\pi$ and is defined as

$$r_\pi = \frac{\beta}{i_b}$$  \hspace{1cm} (5.92)

Using Eq. (5.91) gives

$$r_\pi = \frac{\beta}{g_m}$$  \hspace{1cm} (5.93)

Thus $r_\pi$ is directly dependent on $\beta$ and is inversely proportional to the bias current $I_C$. Substituting for $g_m$ in Eq. (5.93) from Eq. (5.87) and replacing $I_C/\beta$ by $I_B$ gives an alternative expression for $r_\pi$,

$$r_\pi = \frac{V_T}{I_B}$$  \hspace{1cm} (5.94)

### 5.6.3 The Emitter Current and the Input Resistance at the Emitter

The total emitter current $i_E$ can be determined from

$$i_E = \frac{I_C}{\alpha} + \frac{i_e}{\alpha}$$

Thus,

$$i_E = I_C + i_e$$  \hspace{1cm} (5.95)

where $I_C$ is equal to $I_C/\alpha$ and the signal current $i_e$ is given by

$$i_e = \frac{i_e}{\alpha} = \frac{I_C}{V_T} v_{be} = \frac{I_C}{V_T}$$  \hspace{1cm} (5.96)

If we denote the small-signal resistance between base and emitter, looking into the emitter, by $r_e$, it can be defined as

$$r_e = \frac{\alpha}{i_e}$$  \hspace{1cm} (5.97)

Using Eq. (5.96) we find that $r_e$, called the **emitter resistance**, is given by

$$r_e = \frac{V_T}{I_e}$$  \hspace{1cm} (5.98)

Comparison with Eq. (5.87) reveals that

$$r_e = \frac{\alpha}{g_m} = \frac{1}{g_m}$$  \hspace{1cm} (5.99)

The relationship between $r_e$ and $r_\pi$ can be found by combining their respective definitions in Eqs. (5.92) and (5.97) as

$$v_{be} = i_f r_e = i_f r_\pi$$
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Thus,

\[ r_x = \left( \frac{i_x}{v_x} \right) r_e \]

which yields

\[ r_x = (\beta + 1) r_e \]  \hspace{1cm} (5.100)

**EXERCISE**

5.37 A BJT having \( \beta = 100 \) is biased at a dc collector current of 1 mA. Find the value of \( g_m, r_e, \) and \( r_\pi \) at the bias point.

Ans. 40 mA/V; 25 Ω; 2.5 kΩ

5.6.4 Voltage Gain

In the preceding section we have established only that the transistor senses the base–emitter signal \( v_{be} \) and causes a proportional current \( g_m v_{be} \) to flow in the collector lead at a high (ideally infinite) impedance level. In this way the transistor is acting as a voltage-controlled current source. To obtain an output voltage signal, we may force this current to flow through a resistor, as is done in Fig. 5.48(a). Then the total collector voltage \( v_C \) will be

\[
\begin{align*}
v_C &= V_C - i_C R_C \\
&= V_C - (i_C + i_R) R_C \\
&= (V_C - i_R R_C) - i_R R_C \\
&= V_C - i_R R_C
\end{align*}
\]  \hspace{1cm} (5.101)

where the voltage \( V_C \) is the dc bias voltage at the collector, and the signal voltage is given by

\[
\begin{align*}
v_I &= -i_R R_C = -g_m v_{be} R_C \\
&= (-g_m R_C) v_{be}
\end{align*}
\]  \hspace{1cm} (5.102)

Thus the voltage gain of this amplifier \( A_v \) is

\[ A_v = \frac{v_I}{v_{be}} = -g_m R_C \]  \hspace{1cm} (5.103)

Here again we note that because \( g_m \) is directly proportional to the collector bias current, the gain will be as stable as the collector bias current is made. Substituting for \( g_m \) from Eq. (5.87) enables us to express the gain in the form

\[ A_v = -\frac{i_C R_C}{V_C} \]  \hspace{1cm} (5.104)

which is identical to the expression we derived in Section 5.3 (Eq. 5.56).

**EXERCISE**

5.38 In the circuit of Fig. 5.48(a), \( V_{CC} \) is adjusted to yield a dc collector current of 1 mA. Let \( V_{CC} = 15 \text{ V} \), \( R_C = 10 \text{ kΩ} \), and \( \beta = 100 \). Find the voltage gain \( v_I/v_{be} \). If \( V_{CC} = 0.005 \text{ sin } \omega t \) volts, find \( v_I(t) \) and \( i_C(t) \).

Ans. \(-400 \text{ V/V}; 5 - 2 \text{ sin } \omega t \text{ volts; } 10 + 2 \text{ sin } \omega t \mu A \)
5.6.5 Separating the Signal and the DC Quantities

The analysis above indicates that every current and voltage in the amplifier circuit of Fig. 5.48(a) is composed of two components: a dc component and a signal component. For instance, \( v_{BE} = V_{BE} + v_{be} \), \( I_C = I_C + i_C \), and so on. The dc components are determined from the dc circuit given in Fig. 5.48(b) and from the relationships imposed by the transistor (Eqs. 5.78 through 5.81). On the other hand, a representation of the signal operation of the BJT can be obtained by eliminating the dc sources, as shown in Fig. 5.50. Observe that since the voltage of an ideal dc supply does not change, the signal voltage across it will be zero. For this reason we have replaced \( V_{CC} \) and \( V_{BE} \) with short circuits. Had the circuit contained ideal dc current sources, these would have been replaced by open circuits. Note, however, that the circuit of Fig. 5.50 is useful only in so far as it shows the various signal currents and voltages; it is not an actual amplifier circuit since the dc bias circuit is not shown.

Figure 5.50 also shows the expressions for the current increments \( i_c \), \( i_b \), and \( i_e \) obtained when a small signal \( v_{be} \) is applied. These relationships can be represented by a circuit. Such a circuit should have three terminals—C, B, and E—and should yield the same terminal currents indicated in Fig. 5.50. The resulting circuit is then equivalent to the transistor as far as small-signal operation is concerned, and thus it can be considered an equivalent small-signal circuit model.

5.6.6 The Hybrid-π Model

An equivalent circuit model for the BJT is shown in Fig. 5.51(a). This model represents the BJT as a voltage-controlled current source and explicitly includes the input resistance looking into the base circuit. The equivalent circuit in (b) represents the BJT as a current-controlled current source (a transconductance amplifier), and that in (b) represents the BJT as a current-controlled current source (a current amplifier).
the base, $r_\pi$. The model obviously yields $i_t = g_m v_{be}$ and $i_e = v_{be}/r_\pi$. Not so obvious, however, is the fact that the model also yields the correct expression for $i_e$. This can be shown as follows:

At the emitter node we have

$$i_e = \frac{v_{be}}{r_\pi} = \frac{g_m v_{be}}{r_\pi} = \frac{v_{be} (1 + \beta)}{r_\pi} = \frac{v_{be}}{r_\pi}$$

A slightly different equivalent circuit model can be obtained by expressing the current of the controlled source ($g_m v_{be}$) in terms of the base current as follows:

$$g_m v_{be} = g_m (1 + \beta) = \frac{v_{be}}{r_\pi}$$

This results in the alternative equivalent circuit model shown in Fig. 5.51(b). Here the transistor is represented as a current-controlled current source, with the control current being $i_b$.

The two models of Fig. 5.51 are simplified versions of what is known as the hybrid-$\pi$ model. This is the most widely used model for the BJT.

It is important to note that the small-signal equivalent circuits of Fig. 5.51 model the operation of the BJT at a given bias point. This should be obvious from the fact that the model parameters $g_m$ and $r_\pi$ depend on the value of the dc bias current $I_C$, as indicated in Fig. 5.51. Finally, although the models have been developed for an npn transistor, they apply equally well to pnp transistors with no change of polarities.

### 5.6.7 The T Model

Although the hybrid-$\pi$ model (in one of its two variants shown in Fig. 5.51) can be used to carry out small-signal analysis of all transistor circuits, there are situations in which an alternative model, shown in Fig. 5.52, is much more convenient. This model, called the T model, is shown in Fig. 5.52.
in two versions in Fig. 5.52. The model of Fig. 5.52(a) represents the BJT as a voltage-controlled current source with the control voltage being $v_{be}$. Here, however, the resistance between base and emitter, looking into the emitter, is explicitly shown. From Fig. 5.52(a) we see clearly that the model yields the correct expressions for $i_c$ and $i_e$. For $i_b$ we note that at the base node we have

$$i_b = \frac{v_{be}}{r_e} - g_m v_{be} = \frac{v_{be}}{r_e} \left( 1 - g_m r_e \right)$$

$$= \frac{v_{be} (1 - \alpha)}{r_e} = \frac{v_{be} \left( 1 - \frac{\beta}{\beta + 1} \right)}{r_e}$$

as should be the case.

If in the model of Fig. 5.52(a) the current of the controlled source is expressed in terms of the emitter current as follows:

$$g_m v_{be} = \alpha i_e$$

we obtain the alternative T model shown in Fig. 5.52(b). Here the BJT is represented as a current-controlled current source but with the control signal being $i_e$.

5.6.8 Application of the Small-Signal Equivalent Circuits

The availability of the small-signal BJT circuit models makes the analysis of transistor amplifier circuits a systematic process. The process consists of the following steps:

1. Determine the dc operating point of the BJT and in particular the dc collector current $I_C$.
2. Calculate the values of the small-signal model parameters: $g_m = I_C / V_T$, $r_e = \beta / g_m$, and $r_e = V_T / I_E = 1 / g_m$.
3. Eliminate the dc sources by replacing each dc voltage source with a short circuit and each dc current source with an open circuit.
4. Replace the BJT with one of its small-signal equivalent circuit models. Although any one of the models can be used, one might be more convenient than the others for the particular circuit being analyzed. This point will be made clearer later in this chapter.
5. Analyze the resulting circuit to determine the required quantities (e.g., voltage gain, input resistance). The process will be illustrated by the following examples.

### EXAMPLE 5.14

We wish to analyze the transistor amplifier shown in Fig. 5.53(a) to determine its voltage gain. Assume $\beta = 100$.

**Solution**

The first step in the analysis consists of determining the quiescent operating point. For this purpose we assume that $v_i = 0$. The dc base current will be

$$I_B = \frac{V_{bb} - V_{be}}{R_{bb}}$$

$$= \frac{3 - 0.7}{100} = 0.023 \text{ mA}$$
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The dc collector current will be

\[ I_C = \beta I_B = 100 \times 0.023 = 2.3 \text{ mA} \]

The dc voltage at the collector will be

\[ V_C = V_{CC} - I_C R_C = +10 - 2.3 \times 3 = +3.1 \text{ V} \]

Since \( V_B \) at +0.7 V is less than \( V_C \), it follows that in the quiescent condition the transistor will be operating in the active mode. The dc analysis is illustrated in Fig. 5.53(b).

Having determined the operating point, we may now proceed to determine the small-signal model parameters:

\[ r_e = \frac{V_T}{I_C} = \frac{25 \text{ mV}}{2.3 \text{ mA}} = 10.8 \Omega \]

\[ g_m = \frac{I_C}{V_T} = \frac{2.3 \text{ mA}}{25 \text{ mV}} = 92 \text{ mA/V} \]

\[ r_s = \frac{R_s}{g_m} = \frac{100}{92} = 1.09 \text{ k}\Omega \]

To carry out the small-signal analysis it is equally convenient to employ either of the two hybrid-\( \pi \) equivalent circuit models of Fig. 5.51. Using the first results in the amplifier equivalent
circuit given in Fig. 5.53(c). Note that no dc quantities are included in this equivalent circuit. It is most important to note that the dc supply voltage \( V_{CC} \) has been replaced by a short circuit in the signal equivalent circuit because the circuit terminal connected to \( V_{CC} \) will always have a constant voltage. That is, the signal voltage at this terminal will be zero. In other words, a circuit terminal connected to a constant dc source can always be considered as a signal ground.

Analysis of the equivalent circuit in Fig. 5.53(c) proceeds as follows:

\[
\text{v}_o = \frac{v_r}{r_e + R_{bb}}
\]

where \( r_e = 1.09 \times 10^{-3} \) ohm.

The output voltage \( v_o \) is given by

\[
v_o = -g_m v_i R_C
\]

\[
= -92 \times 0.011 v_i = 3.04 v_i
\]

Thus the voltage gain will be

\[
A_v = \frac{v_o}{v_i} = 3.04 \text{ V/V}
\]

where the minus sign indicates a phase reversal.

**EXAMPLE 5.15**

To gain more insight into the operation of transistor amplifiers, we wish to consider the waveforms at various points in the circuit analyzed in the previous example. For this purpose assume that \( v_i \) has a triangular waveform. First determine the maximum amplitude that \( v_i \) is allowed to have. Then, with the amplitude of \( v_i \) set to this value, give the waveforms of \( i_B(t), v_{BE}(t), i_C(t), \) and \( v_C(t) \).

**Solution**

One constraint on signal amplitude is the small-signal approximation, which stipulates that \( v_i \) should not exceed about 10 mV. If we take the triangular waveform \( v_i \) to be 20 mV peak-to-peak and work backward, Eq. (5.105) can be used to determine the maximum possible peak of \( v_o \).

\[
\hat{v}_v = \frac{v_{oc}}{0.031} = 91 \text{ V}
\]

To check whether or not the transistor remains in the active mode with \( v_i \) having a peak value \( \hat{v}_v = 0.91 \text{ V} \), we have to evaluate the collector voltage. The voltage at the collector will consist of a triangular wave \( v_i \) superimposed on the dc value \( V_C = 3.1 \text{ V} \). The peak voltage of the triangular waveform will be

\[
\hat{v}_v = \hat{v}_v \times \text{gain} = 0.91 \times 3.04 = 2.77 \text{ V}
\]

It follows that when the output swings negative, the collector voltage reaches a minimum of \( 3.1 - 2.77 = 0.33 \text{ V} \), which is lower than the base voltage by less than 0.4 V. Thus the transistor will remain in the active mode with \( v_i \) having a peak value of 0.91 V. Nevertheless, we will use a somewhat lower value for \( \hat{v}_v \) of approximately 0.8 V, as shown in Fig. 5.54(a), and complete the analysis of this problem. The signal current in the base will be triangular, with a peak value \( I_b \) of

\[
I_b = \frac{\hat{v}_v}{R_{bb} + r_e} = 0.8 \times \frac{91}{100 + 1.09} = 0.008 \text{ mA}
\]
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FIGURE 5.54 Signal waveforms in the circuit of Fig. 5.53.
This triangular-wave current will be superimposed on the quiescent base current $I_B$, as shown in Fig. 5.54(b). The base–emitter voltage will consist of a triangular-wave component superimposed on the dc $V_{BE}$ that is approximately 0.7 V. The peak value of the triangular waveform will be

$$
\hat{V}_{BE} = V_{BE} \frac{E_{t}}{R_{PE}} = 0.8 \times \frac{1.09}{100 + 1.09} = 8.6 \text{ mV}
$$

The total $V_{BE}$ is sketched in Fig. 5.54(c).

The signal current in the collector will be triangular in waveform, with a peak value $I_C$ given by

$$I_C = \beta I_B = 100 \times 0.008 = 0.8 \text{ mA}$$

This current will be superimposed on the quiescent collector current $I_C (=2.3 \text{ mA})$, as shown in Fig. 5.54(d).

Finally, the signal voltage at the collector can be obtained by multiplying $v_i$ by the voltage gain; that is,

$$V_C = 3.04 \times 0.8 = 2.43 \text{ V}$$

Figure 5.54(e) shows a sketch of the total collector voltage $V_C$ versus time. Note the phase reversal between the input signal $v_i$ and the output signal $V_C$.

**EXAMPLE 5.16**

We need to analyze the circuit of Fig. 5.55(a) to determine the voltage gain and the signal waveforms at various points. The capacitor $C$ is a coupling capacitor whose purpose is to couple the signal $v_i$ to the emitter while blocking dc. In this way the dc bias established by $V^+$ and $V^-$ together with $R_E$ and $R_C$ will not be disturbed when the signal $v_i$ is connected. For the purpose of this example, $C$ will be assumed to be very large and ideally infinite—that is, acting as a perfect short circuit at signal frequencies of interest. Similarly, another very large capacitor is used to couple the output signal $v_o$ to other parts of the system.

$$
\begin{align*}
V^+ &= +10 \text{ V} \\
R_E &= 10 \text{ k}\Omega \\
C &= \infty \\
R_C &= 5 \text{ k}\Omega \\
V^- &= -10 \text{ V}
\end{align*}
$$

**FIGURE 5.55** Example 5.16: (a) circuit; (b) dc analysis;
Solution

We shall start by determining the dc operating point as follows (see Fig. 5.55b):

Assuming $\beta = 100$, then $\alpha = 0.99$, and

Thus the transistor is in the active mode. Furthermore, the collector signal can swing from $-5.4$ V to $+0.4$ V (which is $0.4$ V above the base voltage) without the transistor going into saturation. However, a negative $5.8$-V swing in the collector voltage will (theoretically) cause the minimum collector voltage to be $-11.2$ V, which is more negative than the power-supply voltage. It follows that if we attempt to apply an input that results in such an output signal, the transistor will cut off and the negative peaks of the output signal will be clipped off, as illustrated in Fig. 5.56. The waveform in Fig. 5.56, however, is shown to be linear (except for the clipped peak); that is, the effect of the nonlinear $i_C - v_{BE}$ characteristic is not taken into account. This is not correct, since if we are driving the transistor into cutoff at the negative signal peaks, then we will surely be exceeding the small-signal limit, as will be shown later.

Let us now proceed to determine the small-signal voltage gain. Toward that end, we eliminate the dc sources and replace the BJT with its $T$ equivalent circuit of Fig. 5.52(b). Note that because the base is grounded, the $T$ model is somewhat more convenient than the hybrid-$\pi$ model. Nevertheless, identical results can be obtained using the latter.

Figure 5.55(c) shows the resulting small-signal equivalent circuit of the amplifier. The model parameters are

\[
\alpha = 0.99
\]

\[
\frac{r_e V_I}{I_E} = \frac{25 \text{ mV}}{0.93 \text{ mA}} = 27 \Omega
\]
Analysis of the circuit in Fig. 5.55(c) to determine the output voltage $v_o$ and hence the voltage gain $v_o/v_i$ is straightforward and is given in the figure. The result is

$$A_v = \frac{v_o}{v_i} = 183.3 \text{ V/V}$$

Note that the voltage gain is positive, indicating that the output is in phase with the input signal. This property is due to the fact that the input signal is applied to the emitter rather than to the base, as was done in Example 5.14. We should emphasize that the positive gain has nothing to do with the fact that the transistor used in this example is of the $pnp$ type.

Returning to the question of allowable signal magnitude, we observe from Fig. 5.55(c) that $v_{eb} = v_i$. Thus, if small-signal operation is desired (for linearity), then the peak of $v_i$ should be limited to approximately 10 mV. With $v_i$ set to this value, as shown for a sine-wave input in Fig. 5.57,
the peak amplitude at the collector, $\hat{V}_c$, will be

$$\hat{V}_c = 183.3 \times 0.01 = 1.833 \text{ V}$$

and the total instantaneous collector voltage $v_c(t)$ will be as depicted in Fig. 5.57(b).

**EXERCISE**

5.39 To increase the voltage gain of the amplifier analyzed in Example 5.16, the collector resistance $R_C$ is increased to 7.5 $k\Omega$. Find the new values of $V_C$, $A_v$, and the peak amplitude of the output sine wave corresponding to an input sine wave $v_i$ of 10 mV peak.

**Ans.** -3.1 V; 275 V/V; 2.75 V

5.6.9 Performing Small-Signal Analysis Directly on the Circuit Diagram

In most cases one should explicitly replace each BJT with its small-signal model and analyze the resulting circuit, as we have done in the examples above. This systematic procedure is particularly recommended for beginning students. Experienced circuit designers, however, often perform a first-order analysis directly on the circuit. Figure 5.55(d) illustrates this process for the circuit we have just analyzed. The reader is urged to follow this direct analysis procedure (the steps are numbered). Observe that the equivalent circuit model is implicitly utilized; we are only saving the step of redrawing the circuit with the BJT replaced with its model. Direct analysis, however, has an additional very important benefit: It provides insight regarding the signal transmission through the circuit. Such insight can prove invaluable in design, particularly at the stage of selecting a circuit configuration appropriate for a given application.

5.6.10 Augmenting the Small-Signal Models to Account for the Early Effect

The Early effect, discussed in Section 5.2, causes the collector current to depend not only on $v_{be}$ but also on $v_{ce}$. The dependence on $v_{ce}$ can be modeled by assigning a finite output resistance to the controlled current-source in the hybrid-$\pi$ model, as shown in Fig. 5.58. The output resistance $r_o$ was defined in Eq. (5.37); its value is given by

$$r_o = \frac{V_A}{I_C}$$

where $V_A$ is the Early voltage and $V_C$ and $I_C$ are the coordinates of the dc bias point. Note that in the models of Fig. 5.58 we have renamed $v_{be}$ as $v_{\pi}$, in order to conform with the literature.

**FIGURE 5.58** The hybrid-$\pi$ small-signal model, in its two versions, with the resistance $r_o$ included.
The question arises as to the effect of $r_o$ on the operation of the transistor as an amplifier. In amplifier circuits in which the emitter is grounded (as in the circuit of Fig. 5.53), $r_o$ simply appears in parallel with $R_e$. Thus, if we include $r_o$ in the equivalent circuit of Fig. 5.53(c), for example, the output voltage $v_o$ becomes

$$v_o = v_{be} + (R_e + r_e)$$

Thus the gain will be somewhat reduced. Obviously if $r_o \gg R_e$, the reduction in gain will be negligible, and one can ignore the effect of $r_o$. In general, in such a configuration $r_e$ can be neglected if it is greater than $10R_e$.

When the emitter of the transistor is not grounded, including $r_o$ in the model can complicate the analysis. We will make comments regarding $r_o$ and its inclusion or exclusion on frequent occasions throughout the book. We should also note that in integrated-circuit BJT amplifiers, $r_o$ plays a dominant role, as will be seen in Chapter 6. Of course, if one is performing an accurate analysis of an almost-final design using computer-aided analysis, then $r_e$ can be easily included (see Section 5.11).

Finally, it should be noted that either of the $T$ models in Fig. 5.52 can be augmented to account for the Early effect by including $r_o$ between collector and emitter.

### 5.6.11 Summary

The analysis and design of BJT amplifier circuits is greatly facilitated if the relationships between the various small-signal model parameters are at your fingertips. For easy reference, these are summarized in Table 5.4. Over time, however, we expect the reader to be able to recall these from memory.

#### EXERCISE

5.40 The transistor in Fig. E5.40 is biased with a constant current source $I = 1\ mA$ and has $\beta = 100$ and $V_T = 100\ V$. (a) Find the dc voltages at the base, emitter, and collector. (b) Find $g_m$, $r_e$, and $r_o$. (c) If terminal $Z$ is connected to ground, $X$ to a signal source $v_s$ with a source resistance $R_s = 2\ k\ \Omega$, and $Y$ to an $8\ k\ \Omega$ load resistance, use the hybrid-$\pi$ model of Fig. 5.58(a), to draw the small-signal equivalent circuit of the amplifier. (Note that the current source $I$ should be replaced with an open circuit.) Calculate the overall voltage gain $v_y/v_s$. If $r_o$ is neglected what is the error in estimating the gain magnitude? (Note: An infinite capacitance is used to indicate that the capacitance is sufficiently large that it acts as a short circuit at all signal frequencies of interest. However, the capacitor still blocks dc.)

Ans. (a) $-0.1\ V$, $-0.8\ V$, $+2\ V$; (b) $40\ mA/V$, $2.5\ k\ \Omega$, $100\ k\ \Omega$; (c) $-77\ V/V$, $+3.9\%$
### TABLE 5.4  Small-Signal Models of the BJT

#### Hybrid-$\pi$ Model

<table>
<thead>
<tr>
<th>Version</th>
<th>Symbol</th>
<th>Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>$(g_m \alpha)$</td>
<td><img src="image" alt="Hybrid-$\pi$ Model" /></td>
<td>$r_e = \alpha g_m$, $r_s = \beta g_m$</td>
</tr>
<tr>
<td>$(\beta i_b)$</td>
<td><img src="image" alt="Hybrid-$\pi$ Model" /></td>
<td>$r_e = \beta i_b$, $r_s = \frac{V_c}{I_c}$</td>
</tr>
</tbody>
</table>

#### T Model

<table>
<thead>
<tr>
<th>Version</th>
<th>Symbol</th>
<th>Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>$(g_m \alpha)$</td>
<td><img src="image" alt="T Model" /></td>
<td>$r_e = \alpha g_m$, $r_s = \beta g_m$</td>
</tr>
<tr>
<td>$(\alpha i_b)$</td>
<td><img src="image" alt="T Model" /></td>
<td>$r_e = \alpha i_b$, $r_s = \frac{V_c}{I_c}$</td>
</tr>
</tbody>
</table>

#### Model Parameters in Terms of DC Bias Currents

- $g_m = \frac{I_c}{V_c}$
- $r_e = \frac{V_C}{I_C} = \alpha \left( \frac{V_C}{I_C} \right)$
- $r_s = \frac{V_C}{I_C} = \beta \left( \frac{V_C}{I_C} \right)$
- $r = \frac{V_C}{I_C}$

#### In Terms of $g_m$

- $r_e = \alpha g_m$, $r_s = \beta g_m$

#### In Terms of $r_e$

- $g_m = \frac{V_C}{I_C}$
- $r_s = (\beta + 1) r_e$
- $r_e + \frac{1}{r_e} = \frac{1}{r_e}

#### Relationships Between $\alpha$ and $\beta$

- $\beta = \frac{\alpha}{1-\alpha}$
- $\alpha = \frac{\beta}{\beta + 1}$
- $\beta + 1 = \frac{1}{1-\alpha}$
5.7 SINGLE-STAGE BJT AMPLIFIERS

We have studied the large-signal operation of BJT amplifiers in Section 5.3 and identified the region over which a properly biased transistor can be operated as a linear amplifier for small signals. Methods for dc biasing the BJT were studied in Section 5.5, and a detailed study of the small-signal amplifier operation was presented in Section 5.6. We are now ready to consider practical transistor amplifiers, and we will do so in this section for circuits suitable for discrete-circuit fabrication. The design of integrated-circuit BJT amplifiers will be studied in Chapter 6.

There are basically three configurations for implementing single-stage BJT amplifiers: the common-emitter, the common-base, and the common-collector configurations. All three are studied below, utilizing the same basic structure with the same biasing arrangement.

5.7.1 The Basic Structure

Figure 5.59 shows the basic circuit that we shall utilize to implement the various configurations of BJT amplifiers. Among the various biasing schemes possible for discrete BJT amplifiers (Section 5.5), we have selected, for simplicity and effectiveness, the one employing constant-current biasing. Figure 5.59 indicates the dc currents in all branches and the dc voltages at all nodes. We should note that one would want to select a large value for $R_B$ in order to keep the input resistance at the base large. However, we also want to limit the dc voltage drop across $R_B$ and even more importantly the variability of this dc voltage resulting from the variation in $\beta$ values among transistors of the same type. The dc voltage $V_B$ determines the allowable signal swing at the collector.

**FIGURE 5.59** Basic structure of the circuit used to realize single-stage, discrete-circuit BJT amplifier configurations.
5.7 Characterizing BJT Amplifiers

As we begin our study of BJT amplifier circuits, it is important to know how to characterize the performance of amplifiers as circuit building blocks. An introduction to this subject was presented in Section 1.5. However, the material of Section 1.5 was limited to unilateral amplifiers. A number of the amplifier circuits we shall study in this book are not unilateral; that is, they have internal feedback that may cause their input resistance to depend on the load resistance. Similarly, internal feedback may cause the output resistance to depend on the value of the resistance of the signal source feeding the amplifier.

To accommodate nonunilateral amplifiers, we present in Table 5.5 a general set of parameters and equivalent circuits that we will employ in characterizing and comparing transistor amplifiers. A number of remarks are in order:

1. The amplifier in Table 5.5 is shown fed with a signal source having an open-circuit voltage $v_{\text{sig}}$ and an internal resistance $R_{\text{sig}}$. These can be the parameters of an actual signal source or the Thévenin equivalent of the output circuit of another amplifier stage preceding the one under study in a cascade amplifier. Similarly, $R_L$ can be an actual load resistance or the input resistance of a succeeding amplifier stage in a cascade amplifier.

Exercise 5.41

Consider the circuit of Fig. 5.59 for the case $V_{\text{cc}} = V_{\text{ee}} = 10\,\text{V}$, $I = 1\,\text{mA}$, $R_B = 100\,\text{k}\Omega$, $R_C = 8\,\text{k}\Omega$, and $\beta = 100$. Find all dc currents and voltages. What are the allowable signal swings at the collector in both directions? How do these values change as $\beta$ is changed to 50? To 200? Evaluate the values of the BJT small-signal parameters at the bias point (with $\beta = 100$). The Early voltage $V_A = 100\,\text{V}$.

Ans. See Fig. E5.41. Signal swing: for $\beta = 100$, $+8\,\text{V}$, $-3.4\,\text{V}$; for $\beta = 50$, $+8\,\text{V}$, $-4.4\,\text{V}$; for $\beta = 200$, $+8\,\text{V}$, $-2.9\,\text{V}$.

![Figure E5.41](image-url)
<table>
<thead>
<tr>
<th>Circuit</th>
<th>Definitions</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image" alt="Table 5.5" /></td>
<td><img src="image" alt="Definitions" /></td>
</tr>
</tbody>
</table>

### TABLE 5.5 Characteristic Parameters of Amplifiers

- **Open-circuit voltage gain**: $A_{oc} = \frac{v_o}{v_i}$
- **Voltage gain**: $A_v = \frac{v_o}{v_i}$
- **Current gain**: $A_i = \frac{i_o}{i_i}$
- **Short-circuit transconductance**: $g_m = \frac{i_o}{v_i}$
- **Output resistance of amplifier proper**: $R_o = \frac{i_o}{v_i}$
5.7 SINGLE-STAGE BJT AMPLIFIERS

- **Output resistance:**
  \[ R_{out} = \frac{v_x}{i_x} \]

- **Open-circuit overall voltage gain:**
  \[ G_v = \frac{v_o}{v_{eq}} \]

- **Overall voltage gain:**
  \[ G_v = \frac{v_o}{v_{in}} \]

**Equivalent Circuits**

- **A:**

- **B:**

- **C:**

(Continued)
CHAPTER 5  BIPOLAR JUNCTION TRANSISTORS (BJTs)

2. Parameters \( R_i \), \( R_o \), \( A_v \), \( A_{io} \), and \( G_m \) pertain to the amplifier proper; that is, they do not depend on the values of \( R_{sig} \) and \( R_L \). By contrast, \( R_{in} \), \( R_{out} \), \( A_v \), \( A_{io} \), \( G_{vo} \), and \( G_{vo} \) may depend on one or both of \( R_{sig} \) and \( R_L \). Also, observe the relationships of related pairs of these parameters; for instance, \( A_v = \frac{R_o}{R_o + R_{out}} \) and \( A_{io} = \frac{R_i}{R_i + R_{in}} \).

3. As mentioned above, for nonunilateral amplifiers, \( R_{in} \) may depend on \( R_L \), and \( R_{out} \) may depend on \( R_{sig} \). One such amplifier circuit is studied in Section 5.7.6. No such dependencies exist for unilateral amplifiers, for which \( R_{in} = R_i \) and \( R_{out} = R_o \).

4. The loading of the amplifier on the signal source is determined by the input resistance \( R_{in} \). The value of \( R_{in} \) determines the current \( i_i \) that the amplifier draws from the signal source. It also determines the proportion of the signal \( v_{sig} \) that appears at the input of the amplifier proper, that is, \( v_i \).

5. When evaluating the gain \( A_v \) from the open-circuit value \( A_{io} \), \( R_i \) is the output resistance to use. This is because \( A_v \) is based on feeding the amplifier with an ideal voltage signal \( v_i \). This should be evident from Equivalent Circuit A in Table 5.5. On the other hand, if we are evaluating the overall voltage gain \( G_v \) from its open-circuit value \( G_{vo} \), the output resistance to use is \( R_{out} \). This is because \( G_v \) is based on feeding the amplifier with \( v_{sig} \), which has an internal resistance \( R_{sig} \). This should be evident from Equivalent Circuit C in Table 5.5.

6. We urge the reader to carefully examine and reflect on the definitions and the six relationships presented in Table 5.5. Example 5.17 should help in this regard.

**TABLE 5.5** (Continued)

<table>
<thead>
<tr>
<th>Relationships</th>
</tr>
</thead>
<tbody>
<tr>
<td>( v_i = \frac{R_o}{R_o + R_{out}} )</td>
</tr>
<tr>
<td>( A_v = \frac{R_o}{R_o + R_{out}} )</td>
</tr>
<tr>
<td>( A_{io} = \frac{R_i}{R_i + R_{in}} )</td>
</tr>
<tr>
<td>( G_v = \frac{R_o}{R_o + R_{out}} A_v )</td>
</tr>
<tr>
<td>( G_{vo} = \frac{R_i}{R_i + R_{in}} A_{io} )</td>
</tr>
<tr>
<td>( G_m = \frac{R_i}{R_i + R_{in}} )</td>
</tr>
</tbody>
</table>

2. Parameters \( R_i \), \( R_o \), \( A_v \), \( A_{io} \), and \( G_m \) pertain to the amplifier proper; that is, they do not depend on the values of \( R_{sig} \) and \( R_L \). By contrast, \( R_{in} \), \( R_{out} \), \( A_v \), \( A_{io} \), \( G_{vo} \), and \( G_{vo} \) may depend on one or both of \( R_{sig} \) and \( R_L \). Also, observe the relationships of related pairs of these parameters; for instance, \( R_{in} = R_{in} \) and \( R_{out} = R_{out} \).

3. As mentioned above, for nonunilateral amplifiers, \( R_{in} \) may depend on \( R_L \), and \( R_{out} \) may depend on \( R_{sig} \). One such amplifier circuit is studied in Section 5.7.6. No such dependencies exist for unilateral amplifiers, for which \( R_{in} = R_i \) and \( R_{out} = R_o \).

4. The loading of the amplifier on the signal source is determined by the input resistance \( R_{in} \). The value of \( R_{in} \) determines the current \( i_i \) that the amplifier draws from the signal source. It also determines the proportion of the signal \( v_{sig} \) that appears at the input of the amplifier proper, that is, \( v_i \).

5. When evaluating the gain \( A_v \) from the open-circuit value \( A_{io} \), \( R_i \) is the output resistance to use. This is because \( A_v \) is based on feeding the amplifier with an ideal voltage signal \( v_i \). This should be evident from Equivalent Circuit A in Table 5.5. On the other hand, if we are evaluating the overall voltage gain \( G_v \) from its open-circuit value \( G_{vo} \), the output resistance to use is \( R_{out} \). This is because \( G_v \) is based on feeding the amplifier with \( v_{sig} \), which has an internal resistance \( R_{sig} \). This should be evident from Equivalent Circuit C in Table 5.5.

6. We urge the reader to carefully examine and reflect on the definitions and the six relationships presented in Table 5.5. Example 5.17 should help in this regard.

**EXAMPLE 5.17**

A transistor amplifier is fed with a signal source having an open-circuit voltage \( v_{sig} \) of 10 mV and an internal resistance \( R_{sig} \) of 100 k\( \Omega \). The voltage \( v_i \) at the amplifier input and the output voltage \( v_o \) are measured both without and with a load resistance \( R_L = 10 \, \text{k}\( \Omega \) connected to the amplifier output. The measured results are as follows:

<table>
<thead>
<tr>
<th>( v_i ) (mV)</th>
<th>( v_o ) (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Without ( R_L )</td>
<td>9  90</td>
</tr>
<tr>
<td>With ( R_L ) connected</td>
<td>8  70</td>
</tr>
</tbody>
</table>

Find all the amplifier parameters.
Solution
First, we use the data obtained for $R_L = \infty$ to determine

$$A_v = \frac{90}{9} = 10 \text{ V/V}$$

and

$$G_{ve} = \frac{90}{10} = 9 \text{ V/V}$$

Now, since

$$G_{ve} = \frac{R_I}{R_L + R_{oA}}$$

$$9 = \frac{R_I}{R_L + 100} \times 10$$

which gives

$$R_I = 900 \text{ k}\Omega$$

Next, we use the data obtained when $R_L = 10 \text{ k}\Omega$ is connected to the amplifier output to determine

$$A_v = \frac{70}{10} = 8.75 \text{ V/V}$$

and

$$G_{ve} = \frac{70}{10} = 7 \text{ V/V}$$

The values of $A_v$ and $A_{ov}$ can be used to determine $R_I$ as follows:

$$A_v = A_{ov} \frac{R_L}{R_L + R_{oA}}$$

$$8.75 = 10 \frac{10}{10 + R_{oA}}$$

which gives

$$R_{oA} = 1.43 \text{ k}\Omega$$

Similarly, we use the values of $G_v$ and $G_{ve}$ to determine $R_{oA}$ from

$$G_v = G_{ve} \frac{R_L}{R_L + R_{oA}}$$

$$7 = 9 \frac{10}{10 + R_{oA}}$$

resulting in

$$R_{oA} = 2.86 \text{ k}\Omega$$

The value of $R_{in}$ can be determined from

$$\frac{v_i}{v_{in}} = \frac{R_o}{R_{oA} + R_{in}}$$
Thus,\[
\frac{8}{10} = \frac{R_x}{R_{in} + 100}
\]
which yields\[R_x = 400 \text{ k}\Omega\]
The short-circuit transconductance $G_m$ can be found as follows:\[G_m = \frac{A_{io}}{R_E} = \frac{10}{14.3} = 7 \text{ mA/V}\]
and the current gain $A_i$ can be determined as follows:\[A_i = \frac{v_o/R_E}{v_i/R_m} = \frac{v_o}{v_i} R_m
\]
\[= A R_E = 8.75 \times \frac{400}{10} = 350 \text{ A/A}\]
Finally, we determine the short-circuit current gain $A_{is}$ as follows. From Equivalent Circuit A, the short-circuit output current is\[i_{osc} = A_i v_i/R_s\] (5.107)
However, to determine $v_i$ we need to know the value of $R_x$, obtained with $R_L = 0$. Toward this end, note that from Equivalent Circuit C, the output short-circuit current can be found as\[i_{osc} = G_{vo} v_{sig}/R_{out}\] (5.108)
Now, equating the two expressions for $i_{osc}$ and substituting for $G_{vo}$ by\[G_{vo} = \frac{R_{in}}{R_s + R_{sig}} A_{vo}\]
and for $v_{sig}$ from\[v_{sig} = \frac{R_{in} R_{out}}{R_{in} + R_{sig}} A_{vo}\]
results in\[R_{in} R_{out} = R_{in} \left( 1 + \frac{R_{in} R_{out}}{R_s} \right) - 1
\]
\[= 81.8 \text{ k}\Omega\]
We now can use\[i_{osc} = A_{is} i_i R_{in}/R_s
\] to obtain\[A_{is} = \frac{i_{osc}}{i_i} = 10 \times 81.8/1.43 = 572 \text{ A/A}\]
5.73 The Common-Emitter (CE) Amplifier

The CE configuration is the most widely used of all BJT amplifier circuits. Figure 5.60(a) shows a CE amplifier implemented using the circuit of Fig. 5.59. To establish a signal ground (or an ac ground, as it is sometimes called) at the emitter, a large capacitor $C_{E}$, usually in the $\mu$F or tens of $\mu$F range, is connected between emitter and ground. This capacitor

![Diagram of a common-emitter amplifier using the structure of Fig. 5.59.](image)

![Equivalent circuit obtained by replacing the transistor with its hybrid-$\pi$ model.](image)

**EXERCISE**

5.42 Refer to the amplifier of Example 5.17. (a) If $R_{S}$ is doubled, find the values for $R_{i}$, $G_{m}$, and $R_{o}$. (b) Repeat for $R_{L}$ doubled (but $R_{S}$ unchanged; i.e., 100 k$\Omega$). (c) Repeat for both $R_{S}$ and $R_{L}$ doubled.

*Ans.* (a) 400 k$\Omega$, 5.83 V/V, 4.03 k$\Omega$; (b) 538 k$\Omega$, 7.87 V/V, 2.86 k$\Omega$; (c) 538 k$\Omega$, 6.8 V/V, 4.03 k$\Omega$
is required to provide a very low impedance to ground (ideally, zero impedance; i.e., in effect, a short circuit) at all signal frequencies of interest. In this way, the emitter signal current passes through \( C_E \) to ground and thus bypasses the output resistance of the current source \( I \) (and any other circuit component that might be connected to the emitter); hence \( C_E \) is called a bypass capacitor. Obviously, the lower the signal frequency, the less effective the bypass capacitor becomes. This issue will be studied in Section 5.9. For our purposes here we shall assume that \( C_E \) is acting as a perfect short circuit and thus is establishing a zero signal voltage at the emitter.

In order not to disturb the dc bias currents and voltages, the signal to be amplified, shown as a voltage source \( v_{sig} \) with an internal resistance \( R_{sig} \), is connected to the base through a large capacitor \( C_C \), known as a coupling capacitor, is required to act as a perfect short circuit at all signal frequencies of interest while blocking dc. Here again we shall assume this to be the case and defer discussion of imperfect signal coupling as a result of the rise of the impedance of \( C_C \) at low frequencies to Section 5.9. At this point we should point out that in situations where the signal source can provide a dc path for the dc base current \( I_B \) without significantly changing the bias point we may connect the source directly to the base, thus dispensing with \( R_B \) as well as \( C_C \). Eliminating \( R_B \) has the added beneficial effect of raising the input resistance of the amplifier.

The voltage signal resulting at the collector, \( v_C \), is coupled to the load resistance \( R_L \) via another coupling capacitor \( C_C \). We shall assume that \( C_C \) also acts a perfect short circuit at all signal frequencies of interest; thus the output voltage \( v_c = v_{o} \). Note that \( R_L \) can be an actual load resistor to which the amplifier is required to provide its output voltage signal, or it can be the input resistance of a subsequent amplifier stage in cases where more than one stage of amplification is needed. (We will study multistage amplifiers in Chapter 7).

To determine the terminal characteristics of the CE amplifier, that is, its input resistance, voltage gain, and output resistance, we replace the BJT with its hybrid-\( \pi \) small-signal model. The resulting small-signal equivalent circuit of the CE amplifier is shown in Fig. 5.60(b). We observe at the outset that this amplifier is unilateral and thus \( R_{in} = R_i \) and \( R_{out} = R_o \). Analysis of this circuit is straightforward and proceeds in a step-by-step manner, from the signal source to the amplifier load. At the amplifier input we have

\[
R_{in} = \frac{R_B}{I} = R_i \| R_{o}
\]

where \( R_{in} \) is the input resistance looking into the base. Since the emitter is grounded,

\[
R_{\beta} = r_{\pi}
\]

Normally, we select \( R_E \gg r_{\pi} \), with the result that

\[
R_{\beta} \approx r_{\pi}
\]

Thus, we note that the input resistance of the CE amplifier will typically be a few kilohms, which can be thought of as low to moderate. The fraction of source signal \( v_{sig} \) that appears across the input terminals of the amplifier proper can be found from

\[
v_i = v_{sig} \frac{R_B}{R_i + R_{o}} = v_{sig} \frac{(R_B)(r_{\pi})}{(R_i + r_{\pi}) + R_{sig}}
\]

where

\[
R_{o} = \frac{R_B}{I}
\]

and

\[
R_{in} = R_i \| R_{o}
\]
which for \( R_B \gg r_e \) becomes

\[
v_i = v_i_0 - \frac{r_p}{r_e + R_\text{in}}
\]  
(5.114)

Next we note that

\[
v_o = v_i
\]  
(5.115)

At the output of the amplifier we have

\[
v_o = -g_m v_i (r_e \parallel R_L)
\]

Replacing \( v_o \) by \( v_i \) we can write for the voltage gain of the amplifier proper; that is, the voltage gain from base to collector,

\[
A_v = -g_m (r_e \parallel R_L)
\]  
(5.116)

This equation simply says that the voltage gain from base to collector is found by multiplying \( g_m \) by the total resistance between collector and ground. The open-circuit voltage gain \( A_{vo} \) can be obtained by setting \( R_L = \infty \) in Eq. (5.116); thus,

\[
A_{vo} = -g_m r_e
\]  
(5.117)

from which we note that the effect of \( r_o \) is simply to reduce the gain, usually only slightly since typically \( r_e \gg R_L \), resulting in

\[
A_v = -g_m R_C
\]  
(5.118)

The output resistance \( R_{out} \) can be found from the equivalent circuit of Fig. 5.60(b) by looking back into the output terminal while short-circuiting the source \( v_i_0 \). Since this will result in \( v_o = 0 \), we see that

\[
R_{out} = R_C \parallel r_e
\]  
(5.119)

Thus \( r_e \) reduces the output resistance of the amplifier, again usually only slightly since typically \( r_e \gg R_C \) and

\[
R_{out} \approx R_C
\]  
(5.120)

Recalling that for this unilateral amplifier \( R_L = R_{out} \), we can utilize \( A_v \) and \( r_e \) to obtain the voltage gain \( A_v \) corresponding to any particular \( R_L \),

\[
A_v = A_v \frac{R_L}{R_L + R_e}
\]

The reader can easily verify that this approach does in fact lead to the expression for \( A_v \) in Eq. (5.116), which we have derived directly.

The overall voltage gain from source to load, \( G_v \), can be obtained by multiplying \( (v_i/v_i_0) \) from Eq. (5.114) by \( A_v \) from Eq. (5.116),

\[
G_v = \frac{(R_B \parallel r_e)}{(R_B \parallel r_e) + R_\text{in}} g_m (r_e \parallel R_L)
\]  
(5.121)
For the case \( R_s \gg r_e \), this expression simplifies to
\[
G_v = \frac{\beta R_c (R_e || r_e)}{r_e + R_m} \tag{5.122}
\]
From this expression we note that if \( R_s \gg r_e \), the overall gain will be highly dependent on \( \beta \).
This is not a desirable property since \( \beta \) varies considerably between units of the same transistor type. At the other extreme, if \( R_s \ll r_e \), we see that the expression for the overall voltage gain reduces to
\[
G_v = -g_m (R_c || R_e || r_e) \tag{5.123}
\]
which is the gain \( A_v \); in other words, when \( R_s \) is small, the overall voltage gain is almost equal to the gain of the CE circuit proper, which is independent of \( \beta \). Typically a CE amplifier can realize a voltage gain on the order of a few hundred, which is very significant. It follows that the CE amplifier is used to realize the bulk of the voltage gain required in a given amplifier design problem. Unfortunately, however, as we shall see in Section 5.9, the high-frequency response of the CE amplifier can be rather limited.

Before leaving the CE amplifier, we wish to evaluate its short-circuit current gain, \( A_{is} \).
This can be easily done by referring to the amplifier equivalent circuit in Fig. 5.60(b). When \( R_L \) is short circuited, the current through it will be equal to 
\[
-i_{os} = -g_m v_{\pi}
\]
Since \( v_{\pi} \) is related to \( i_i \) by
\[
v_{\pi} = v_i = i_i R_{in}
\]
the short-circuit current gain can be found as
\[
A_{is} = \frac{i_{os}}{i_i} = -g_m R_{in} \tag{5.124}
\]
Substituting \( R_{in} = R_b || r_\pi \), we can see that in the case \( R_s \gg r_e \), \( |A_{is}| \) reduces to \( \beta \), which is to be expected since \( \beta \) is, by definition, the short-circuit current gain of the common-emitter configuration.

In conclusion, the common-emitter configuration can provide large voltage and current gains, but \( R_{in} \) is relatively low and \( R_{out} \) is relatively high.

**EXERCISE 5.43**
Consider the CE amplifier of Fig. 5.60(a) when biased as in Exercise 5.41. In particular, refer to Fig. E5.41 for the bias currents and the values of the elements of the BJT model at the bias point. Evaluate \( R_{in} \) (without and with \( R_b \) taken into account), \( A_{v0} \) (without and with \( r_e \) taken into account), \( A_{v1} \) (without and with \( R_c \) taken into account). For \( R_s = 5 \, \text{k} \Omega \), find \( A_v \). If \( R_s = 5 \, \text{k} \Omega \), find the overall voltage gain \( G_v \). If the sine-wave \( v_{\pi} \) is to be limited to 5 mV peak, what is the maximum allowed peak amplitude of \( i_{os} \) and the corresponding peak amplitude of \( v_o \)?

**Ans.**
2.5 kΩ, 2.4 kΩ; –320 V/V, –296 V/V; 8 kΩ, 7.4 kΩ; –100 A/A, –98 A/A; –119 V/V, –39 V/V; 15 mV, 0.6 V
5.7.4 The Common-Emitter Amplifier with an Emitter Resistance

Including a resistance in the signal path between emitter and ground, as shown in Fig. 5.61(a), can lead to significant changes in the amplifier characteristics. Thus such a resistor can be utilized by the designer as an effective design tool for tailoring the amplifier characteristics to fit the design requirements.

**FIGURE 5.61** (a) A common-emitter amplifier with an emitter resistance $R_e$. (b) Equivalent circuit obtained by replacing the transistor with its T model.
Analysis of the circuit in Fig. 5.61(a) can be performed by replacing the BJT with one of its small-signal models. Although any one of the models of Figs. 5.51 and 5.52 can be used, the most convenient for this application is one of the two T models. This is because we have a resistance $R_e$ in the emitter that will appear in series with the emitter resistance $r_e$ of the T model and can thus be added to it, simplifying the analysis considerably. In fact, whenever there is a resistance in the emitter lead, the T model should prove more convenient to use than the hybrid-$\pi$ model.

Replacing the BJT with the T model of Fig. 5.52(b) results in the amplifier small-signal equivalent-circuit model shown in Fig. 5.61(b). Note that we have not included the BJT output resistance $r_o$; including $r_o$ complicates the analysis considerably. Since for the discrete amplifier at hand it turns out that the effect of $r_o$ on circuit performance is small, we shall not include it in the analysis. This is not the case, however, for the IC version of this circuit, and we shall indeed take $r_e$ into account in the analysis in Chapter 6.

To determine the amplifier input resistance $R_{in}$, we note from Fig. 5.61(b) that $R_{in}$ is the parallel equivalent of $R_B$ and the input resistance at the base $R_{ib}$.

$$R_{in} = R_B \| R_{ib}$$

(5.125)

The input resistance at the base $R_{ib}$ can be found from

$$R_{ib} = \frac{1}{i_b}$$

where

$$i_b = (1 - \alpha) i_e = \frac{V_i}{\beta + 1}$$

and

$$i_e = \frac{V_i}{r_e + R_e}$$

(5.126)

Thus,

$$R_{ib} = (\beta + 1)(r_e + R_e)$$

(5.127)

This is a very important result. It says that the input resistance looking into the base is $(\beta + 1)$ times the total resistance in the emitter. Multiplication by the factor $(\beta + 1)$ is known as the resistance-reflection rule. The factor $(\beta + 1)$ arises because the base current is $1/(\beta + 1)$ times the emitter current. The expression for $R_{ib}$ in Eq. (5.127) shows clearly that including a resistance $R_e$ in the emitter can substantially increase $R_{ib}$. Indeed the value of $R_{ib}$ is increased by the ratio

$$\frac{R_{ib} \text{ (with } R_e \text{ included)}}{R_{ib} \text{ (without } R_e)} = \frac{(\beta + 1)(r_e + R_e)}{(\beta + 1)r_e} = 1 + \frac{R_e}{r_e} = 1 + \frac{1}{\beta}$$

(5.128)

Thus the circuit designer can use the value of $R_e$ to control the value of $R_{ib}$ and hence $R_{in}$. Of course, for this control to be effective, $R_{ib}$ must be much larger than $R_{in}$; in other words, $R_{ib}$ must dominate the input resistance.

To determine the voltage gain $A_v$, we see from Fig. 5.61(b) that

$$v_o = -i_e (R_e \| R_L)$$

$$= -\alpha i_b (R_e \| R_L)$$

(5.129)
Substituting for \( i_e \) from Eq. (5.126) gives

\[
A_v = \frac{v_o}{v_i} = \frac{\alpha (R_C \parallel R_1)}{r_C + R_e}
\]

Since \( \alpha \approx 1 \),

\[
A_v = \frac{R_C \parallel R_1}{r_C + R_e}
\]

This simple relationship is very useful and is definitely worth remembering: The voltage gain from base to collector is equal to the ratio of the total resistance in the collector to the total resistance in the emitter. This statement is a general one and applies to any amplifier circuit. The open-circuit voltage gain \( A_{o_v} \) can be found by setting \( R_L = \infty \) in Eq. (5.129),

\[
A_{o_v} = -\frac{\alpha R_C}{r_C + R_e}
\]

which can be expressed alternatively as

\[
A_{o_v} = -\frac{\alpha}{1 + g_m R_e}
\]

Including \( R_e \) thus reduces the voltage gain by the factor \( (1 + g_m R_e) \), which is the same factor by which \( R_{ib} \) is increased. This points out an interesting trade-off between gain and input resistance, a trade-off the designer can exercise through the choice of an appropriate value for \( R_e \).

The output resistance \( R_{out} \) can be found from the circuit in Fig. 5.61(b) by inspection:

\[
R_{out} = R_C
\]

At this point we should note that for this amplifier, \( R_{in} = R_i \) and \( R_{out} = R_e \).

The short-circuit current gain \( A_{is} \) can be found from the circuit in Fig. 5.61(b) as follows:

\[
i_o = -\alpha i_e
\]

\[
i_i = v_i / R_{is}
\]

Thus,

\[
A_{is} = -\frac{\alpha R_{is}}{v_i}
\]

Substituting for \( i_e \) from Eq. (5.126) and for \( R_{is} \) from Eq. (5.125),

\[
A_{is} = -\frac{\alpha (R_C \parallel R_1)}{r_C + R_e}
\]

which for the case \( R_b \gg R_e \) reduces to

\[
A_{is} = -\frac{\alpha (R_C \parallel R_1)}{r_C + R_e} = -\beta
\]

the same value as for the CE circuit.
The overall voltage gain from source to load can be obtained by multiplying $A_v$ by

$$G_v = \frac{v_i}{v_{sig}}$$

Substituting for $R_i$ by $R_i || R_{ib}$, assuming that $R_b \gg R_{ib}$, and substituting for $R_A$ from Eq. (5.127) results in

$$G_v = \frac{\beta (R_i || R_{ib})}{R_{re} + (\beta + 1)(r_e + R_e)}$$

We note that the gain is lower than that of the CE amplifier because of the additional term $(\beta + 1)g_m$ in the denominator. The gain, however, is less sensitive to the value of $\beta$, a desirable result.

Another important consequence of including the resistance $R_e$ in the emitter is that it enables the amplifier to handle larger input signals without incurring nonlinear distortion. This is because only a fraction of the input signal at the base, $v_i$, appears between the base and the emitter. Specifically, from the circuit in Fig. 5.61(b), we see that

$$V_{out} = \frac{v_i}{r_e + R_e} = \frac{1}{1 + g_m R_e}$$

Thus, for the same $v_i$, the signal at the input terminal of the amplifier, $v_i$, can be greater than for the CE amplifier by the factor $(1 + g_m R_e)$.

To summarize, including a resistance $R_e$ in the emitter of the CE amplifier results in the following characteristics:

1. The input resistance $R_b$ is increased by the factor $(1 + g_m R_e)$.
2. The voltage gain from base to collector, $A_v$, is reduced by the factor $(1 + g_m R_e)$.
3. For the same nonlinear distortion, the input signal $v_i$ can be increased by the factor $(1 + g_m R_e)$.
4. The overall voltage gain is less dependent on the value of $\beta$.
5. The high-frequency response is significantly improved (as we shall see in Chapter 8).

With the exception of gain reduction, these characteristics represent performance improvements. Indeed, the reduction in gain is the price paid for obtaining the other performance improvements. In many cases this is a good bargain; it is the underlying principle for the use of negative feedback. That the resistance $R_e$ introduces negative feedback in the amplifier circuit can be seen by reference to Fig. 5.61(a). If for some reason the collector current increases, the emitter current also will increase, resulting in an increased voltage drop across $R_e$. Thus the emitter voltage rises, and the base-emitter voltage decreases. The latter effect causes the collector current to decrease, counteracting the initially assumed change, an indication of the presence of negative feedback. In Chapter 9, where we shall study negative feedback formally, we will find that the factor $(1 - g_{mre})$ which appears repeatedly, is the "amount of negative feedback" introduced by $R_e$. Finally, we note that the negative feedback action of $R_e$ gives it the name emitter degeneration resistance.

Before leaving this circuit we wish to point out that we have shown a number of the circuit analysis steps directly on the circuit diagram in Fig. 5.61(a). With practice, the reader should be able to do all of the small-signal analysis directly on the circuit, thus dispensing with the task of drawing a complete small-signal equivalent-circuit model.
5.7.5 The Common-Base (CB) Amplifier

By establishing a signal ground on the base terminal of the BJT, a circuit configuration aptly named common-base or grounded-base amplifier is obtained. The input signal is applied to the emitter, and the output is taken at the collector, with the base forming a common terminal between the input and output ports. Figure 5.62(a) shows a CB amplifier based on the circuit of Fig. 5.59. Observe that since both the dc and ac voltages at the base are zero, we have connected the base directly to ground, thus eliminating resistor $R_B$ altogether. Coupling capacitors $C_{C1}$ and $C_{C2}$ perform similar functions to those in the CE circuit.

The small-signal equivalent circuit model of the amplifier is shown in Fig. 5.62(b). Since resistor $R_{s}$ appears in series with the emitter terminal, we have elected to use the T model for the transistor. Although the hybrid-$\pi$ model would yield identical results, the T model is more convenient in this case. We have not included $r_o$. This is because including $r_o$ would complicate the analysis considerably, for it would appear between the output and input of the amplifier. Fortunately, it turns out that the effect of $r_o$ on the performance of a discrete CB amplifier is very small. We will consider the effect of $r_o$ when we study the IC form of the CB amplifier in Chapter 6.

From inspection of the equivalent circuit model in Fig. 5.62(b), we see that the input resistance is

$$R_i = r_e$$

(5.137)

This should have been expected since we are looking into the emitter and the base is grounded. Typically $r_e$ is a few ohms to a few tens of ohms, thus the CB amplifier has a low input resistance.

To determine the voltage gain, we write at the collector node

$$v_C = -\alpha_i (R_e \parallel R_L)$$

and substitute for the emitter current from

$$i_e = \frac{v_i}{r_e}$$

to obtain

$$A_v = \frac{v_o}{v_i} = \frac{\beta (R_e \parallel R_L)}{r_e} = \frac{g_m (R_e \parallel R_L)}{r_e}$$

(5.138)

which except for its positive sign is identical to the expression for $A_v$ for the CE amplifier.

EXERCISE

5.44 Consider the emitter-degenerated CE circuit of Fig. 5.61 when biased as in Exercise 5.41. In particular refer to Fig. E5.41 for the bias currents and for the values of the elements of the BJT model at the bias point. Let the amplifier be fed with a source having $R_{s} = 5 \, \text{k}\Omega$ and let $R_L = 5 \, \text{k}\Omega$. Find the value of $R_L$ that results in $R_{\pi}$ equal to four times the source resistance $R_s$. For this value of $R_L$ find $A_v$, $R_o$, $A_{v_o}$, $G_v$, and $A_{v_o}$. If $v_i$ is to be limited to 5 mV, what is the maximum value $v_{os}$ can have with and without $R_L$ included. Find the corresponding $v_o$.

Ans. $225 \, \Omega$, $-32 \, \text{V/V}$, $8 \, \text{k}\Omega$, $-12.3 \, \text{V/V}$, $-9.8 \, \text{V/V}$, $62.5 \, \text{mV}$, $15 \, \text{mV}$, $0.6 \, \text{V}$
The open-circuit voltage gain $A_{vo}$ can be found from Eq. (5.138) by setting $R_L = \infty$:

$$A_{vo} = \frac{g_m R_C}{1 + g_m R_C}$$

(5.139)

Again, this is identical to $A_{vo}$ for the CE amplifier except that the CB amplifier is noninverting. The output resistance of the CB circuit can be found by inspection from the circuit in FIGURE 5.62.
Fig. 5.62(b) as

\[ R_{\text{in}} = R_c \]

which is similar to the case of the CE amplifier. Here we should note that the CB amplifier with \( r_e \) neglected is unilateral, with the result that \( R_{\text{in}} = R_i \) and \( R_{\text{out}} = R_o \).

The short-circuit current gain \( A_i \) is given by

\[ A_i = \frac{-\alpha i_d}{i_i} = \frac{-\alpha i_e}{i_e} = \alpha \]

which corresponds to our definition of \( \alpha \) as the short-circuit current gain of the CB configuration.

Although the gain of the CB amplifier proper has the same magnitude as that of the CE amplifier, this is usually not the case as far as the overall voltage gain is concerned. The low input resistance of the CB amplifier can cause the input signal to be severely attenuated, specifically

\[ \frac{v_i}{v_{\text{sig}}} = \frac{R_i}{R_{\text{sig}} + R_i} = \frac{r_e}{R_{\text{sig}} + r_e} \]

from which we see that except for situations in which \( R_{\text{sig}} \) is on the order of \( r_e \), the signal transmission factor \( v_i/v_{\text{sig}} \) can be very small. It is useful at this point to mention that indeed one of the applications of the CB circuit is to amplify high-frequency signals that appear on a coaxial cable. To prevent signal reflection on the cable, the CB amplifier is required to have an input resistance equal to the characteristic resistance of the cable, which is usually in the range of 50 \( \Omega \) to 75 \( \Omega \).

The overall voltage gain \( G_v \) of the CB amplifier can be obtained by multiplying the ratio \( v_i/v_{\text{sig}} \) of Eq. (5.141) by \( A_i \) from Eq. (5.138),

\[ G_v = \frac{r_i}{R_{\text{sig}} + R_i} \cdot \frac{\alpha (R_c \parallel R_L)}{R_{\text{sig}} + r_e} \]

Since \( \alpha \approx 1 \), we see that the overall voltage gain is simply the ratio of the total resistance in the collector circuit to the total resistance in the emitter circuit. We also note that the overall voltage gain is almost independent of the value of \( \beta \) (except through the small dependence of \( \alpha \) on \( \beta \)), a desirable property. Observe that for \( R_{\text{sig}} \) of the same order as \( R_i \) and \( R_L \), the gain will be very small.

In summary, the CB amplifier exhibits a very low input resistance \( r_e \) a short-circuit current gain that is nearly unity \( \alpha \), an open-circuit voltage gain that is positive and equal in magnitude to that of the CE amplifier \((g_m R_c)\), and like the CE amplifier, a relatively high output resistance \( R_o \). Because of its very low input resistance, the CB circuit alone is not attractive as a voltage amplifier except in specialized applications, such as the cable amplifier mentioned above. The CB amplifier has excellent high-frequency performance as well, which as we shall see in Chapter 8 makes it useful together with other circuits in the implementation of high-frequency amplifiers. Finally, a very significant application of the CB circuit is as a unity-gain current amplifier or \textbf{current buffer}: It accepts an input signal current at a low input resistance and delivers a nearly equal current at very high output resistance at the collector (the output resistance excluding \( R_e \) and neglecting \( r_e \) is infinite).

We shall study such an application in the context of the IC version of the CB circuit in Chapter 6.
5.76 The Common-Collector (CC) Amplifier or Emitter Follower

The last of the basic BJT amplifier configurations is the common-collector (CC) circuit, a very important circuit that finds frequent application in the design of both small-signal and large-signal amplifiers (Chapter 7) and even in digital circuits (Chapter 11). The circuit is more commonly known by the alternate name emitter follower, the reason for which will shortly become apparent.

An emitter-follower circuit based on the structure of Fig. 5.59 is shown in Fig. 5.63(a). Observe that since the collector is to be at signal ground, we have eliminated the collector resistance $R_C$. The input signal is capacitively coupled to the base, and the output signal is capacitively coupled from the emitter to a load resistance $R_L$.

Since, as far as signals are concerned, resistance $R_L$ is connected in series with the emitter, the T model of the BJT would be the more convenient one to use. Figure 5.63(b) shows the small-signal equivalent circuit of the emitter follower with the BJT replaced by its T model augmented to include $r_o$.

Here it is relatively simple to take $r_o$ into account, and we shall do so. Inspection of the circuit in Fig. 5.63(b) reveals that $r_o$ appears in effect in parallel with $R_L$. Therefore the circuit is redrawn to emphasize this point, and indeed to simplify the analysis, in Fig. 5.63(c).

Unlike the CE and CB circuits we studied above, the emitter-follower circuit is not unilateral; that is, the input resistance depends on $R_L$, and the output resistance depends on $R_{dc}$. Care therefore must be exercised in characterizing the emitter follower. In the following we shall derive expressions for $R_o$, $G_{vo}$, $v_s/v_i$, and $G_{v}$. The expressions that we derive will shed light on the operation and characteristics of the emitter follower. More important than the actual expressions, however, are the methods we use to obtain them. That is what we hope the reader will become proficient in.

Reference to Fig. 5.63(c) reveals that the BJT has a resistance $(r_o || R_L)$ in series with the emitter resistance $r_e$. Thus application of the resistance reflection rule results in the equivalent circuit shown in Fig. 5.64(a). Recall that in reflecting resistances to the base side, we multiply all resistances in the emitter by $(\beta + 1)$, the ratio of $i_e$ to $i_b$. In this way the voltages remain unchanged.

Inspection of the circuit in Fig. 5.64(a) shows that the input resistance at the base, $R_{in}$, is

$$ R_{in} = \left(\beta + 1\right)\left[r_e + \left(\frac{r_o}{R_L}\right)\right] $$

EXERCISES

5.45 Consider the CB amplifier of Fig. 5.62(a) when designed using the BJT and component values specified in Exercise 5.41. Specifically, refer to Fig. E5.41 for the bias quantities and the values of the components of the BJT small-signal model. Let $R_{eq} = R_L = 5 \text{k} \Omega$. Find the values of $R_{eq}$, $A_v$, $R_	ext{in}$, $v_s/v_i$, and $G_{vo}$. To what value should $R_	ext{sig}$ be reduced to obtain an overall voltage gain equal to that found for the CE amplifier in Exercise 5.43, that is, $-39 \text{V/V}$?

Ans. $25 \Omega$; $+320 \text{V/V}$; $+123 \text{V/V}$; $0.005 \text{V/V}$; $0.6 \text{V/V}$; $54 \Omega$.

5.46 It is required to design a CB amplifier for a signal delivered by a 50-Ω coaxial cable. The amplifier is to provide a “proper termination” for the cable and to provide an overall voltage gain of $+100 \text{V/V}$. Specify the value of the bias current $I_b$ and the total resistance in the collector circuit.

Ans. $0.5 \text{mA}$; $10 \text{k} \Omega$.

5.45 Consider the CB amplifier of Fig. 5.62(a) when designed using the BJT and component values specified in Exercise 5.41. Specifically, refer to Fig. E5.41 for the bias quantities and the values of the components of the BJT small-signal model. Let $R_{eq} = R_L = 5 \text{k} \Omega$. Find the values of $R_{eq}$, $A_v$, $R_	ext{in}$, $v_s/v_i$, and $G_{vo}$. To what value should $R_	ext{sig}$ be reduced to obtain an overall voltage gain equal to that found for the CE amplifier in Exercise 5.43, that is, $-39 \text{V/V}$?

Ans. $25 \Omega$; $+320 \text{V/V}$; $+123 \text{V/V}$; $0.005 \text{V/V}$; $0.6 \text{V/V}$; $54 \Omega$.

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Ans. $0.5 \text{mA}$; $10 \text{k} \Omega$.
FIGURE 5.63 (a) An emitter-follower circuit based on the structure of Fig. 5.59. (b) Small-signal equivalent circuit of the emitter follower with the transistor replaced by its T model augmented with $r_o$. (c) The circuit in (b) redrawn to emphasize that $r_o$ is in parallel with $R_L$. This simplifies the analysis considerably.
from which we see that the emitter follower acts to raise the resistance level of $RL$ (or $r_0$ to be exact) by the factor $(\beta + 1)$ and presents to the source the increased resistance. The total input resistance of the follower is

$$R_{in} = R_{B} + (\beta + 1) r_0$$

from which we see that to realize the full effect of the increased $R_{in}$, we have to choose as large a value for the bias resistance $R_B$ as is practical (i.e., from a bias design point of view). Also, whenever possible, we should dispense with $R_B$ altogether and connect the signal source directly to the base (in which case we also dispense with $C_1$).

To find the overall voltage gain $G_v$, we first apply the Thévenin theorem at the input side of the circuit in Fig. 5.64(a) to simplify it to the form shown in Fig. 5.64(b). From the latter circuit we see that $v_o$ can be found by utilizing the voltage divider rule; thus,

$$v_o = \frac{R_B}{R_B + R_{in}} v_{in}$$

(5.144)

We observe that the voltage gain is less than unity; however, for $R_B \gg R_{in}$ and $(\beta + 1)(r_o + (r_0 || R_b) > (R_{in} || R_b)$, it becomes very close to unity. Thus the voltage at the emitter ($v_o$) follows very closely the voltage at the input, which gives the circuit the name emitter follower.

Rather than reflecting the emitter resistance network into the base side, we can do the converse: Reflect the base resistance network into the emitter side. To keep the voltages unchanged, we divide all the base-side resistances by $(\beta + 1)$. This is the dual of the resistance reflection rule. Doing this for the circuit in Fig. 5.63(c) results in the alternate emitter-follower equivalent circuit, shown in Fig. 5.65(a). Here also we can simplify the circuit by applying the Thévenin theorem at the input side, resulting in the circuit in Fig. 5.65(b).
Inspection of the latter reveals that the output voltage and hence can be found by a simple application of the voltage-divider rule, with the result that

\[
G_{v_{o}/v_{i}} = \frac{R_{L}}{R_{L} + R_{B} + r_e + (\beta + 1) R_{L}}
\]  

(5.145)

which, as expected, is identical to the expression in Eq. (5.144) except that both the numerator and denominator of the second factor on the right-hand side have been divided by \((\beta + 1)\). To gain further insight regarding the operation of the emitter follower, let’s simplify this expression for the usual case of \(R_{L} \gg R_{o_{L}}\) and \(r_e \gg R_{L}\). The result is

\[
G_{v_{o}/v_{i}} = \frac{R_{L}}{R_{L} + r_e + R_{L}}
\]  

(5.146)

which clearly indicates that the gain approaches unity when \(R_{o_{L}}/(\beta + 1)\) becomes much smaller than \(R_{L}\) or alternatively when \((\beta + 1)R_{L}\) becomes much larger than \(R_{o_{L}}\). This is the buffering action of the emitter follower, which derives from the fact that the circuit has a short-circuit current that is approximately equal to \((\beta + 1)\).

It is also useful to represent the output of the emitter follower by its Thévenin equivalent circuit. The open-circuit output voltage will be \(G_{v_{o}/v_{i}}\), where \(G_{v_{o}}\) can be obtained from Eq. (5.145) by setting \(R_{L} = \infty\):

\[
G_{v_{o}} = \frac{R_{o_{L}}}{R_{o_{L}} + R_{B} + R_{L} + r_e + r_e + r_e}
\]  

(5.147)
Note that $r_e$ usually is large and the second factor becomes almost unity. The first factor approaches unity for $R_b \gg R_e$. The Thévenin resistance is the output resistance $R_{out}$. It can be determined by inspection of the circuit in Fig. 5.65(b): Reduce $v_{in}$ to zero, “grab hold” of the emitter terminal, and look back into the circuit. The result is

$$R_{out} = r_e \left( r_e + \frac{R_e}{\beta + 1} \right)$$  \hspace{1cm} (5.148)

Usually $r_e$ is much larger than the parallel component between the parentheses and can be neglected, leaving

$$R_{out} = r_e + \frac{R_e}{\beta + 1}$$  \hspace{1cm} (5.149)

Thus the output resistance of the emitter follower is low, again a result of its impedance transformation or buffering action, which leads to the division of $(R_{in} || R_e)$ by $(\beta + 1)$. The Thévenin equivalent circuit of the emitter follower is shown together with the formulas for $G_v$ and $R_{out}$ in Fig. 5.66. This circuit can be used to find $v_o$ and hence $G_v$ for any value of $R_L$.

In summary, the emitter follower exhibits a high input resistance, a low output resistance, a voltage gain that is smaller than but close to unity, and a relatively large current gain. It is therefore ideally suited for applications in which a high-resistance source is to be connected to a low-resistance load—namely, as the last stage or output stage in a multistage amplifier, where its purpose would be not to supply additional voltage gain but rather to give the cascade amplifier a low output resistance. We shall study the design of amplifier output stages in Chapter 7.

Before leaving the emitter follower, the question of the maximum allowed signal swing deserves comment. Since only a small fraction of the input signal appears between the base and the emitter, the emitter follower exhibits linear operation for a large range of input-signal amplitude. There is, however, an absolute upper limit imposed on the value of the output-signal amplitude by transistor cutoff. To see how this comes about, consider the circuit of Fig. 5.63(a) when the input signal is a sine wave. As the input goes negative,
the output $v_o$ will also go negative, and the current in $R_L$ will be flowing from ground into the emitter terminal. The transistor will cut off when this current becomes equal to the bias current $I$. Thus the peak value of $v_o$ can be found from

$$\frac{\hat{V}_o}{R_L} = I$$

or

$$\hat{V}_o = I R_L$$

The corresponding value of $v_{sig}$ will be

$$\hat{V}_{v_{sig}} = I R_L$$

Increasing the amplitude of $v_i$ above this value results in the transistor becoming cut off and the negative peaks of the output-signal waveform being clipped off.

**EXERCISE 5.47** The emitter follower in Fig. 5.63(a) is used to connect a source with $R_{sig} = 10 \, k\Omega$ to a load $R_L = 1 \, k\Omega$. The transistor is biased at $I = 5 \, mA$, utilizes a resistance $R_B = 40 \, k\Omega$ and has $\beta = 100$ and $V_A = 100 \, V$. Find $R_{be}, R_{in}, G_v, G_{vo}$, and $R_{out}$. What is the largest peak amplitude of an output sinusoid that can be used without the transistor cutting off? If in order to limit nonlinear distortion the base–emitter signal voltage is limited to 10 mV peak, what is the corresponding amplitude at the output? What will the overall voltage gain become if $R_L$ is changed to 2 $k\Omega$? To 500 $\Omega$?

**Ans.** 96.7 $k\Omega$; 28.3 $k\Omega$; 0.735 V/V; 0.8 V/V; 84 $\Omega$; 5 V; 1.9 V; 0.768 V/V; 0.685 V/V

### 5.7 Summary and Comparisons

For easy reference and to enable comparisons, we present in Table 5.6 the formulas for determining the characteristic parameters of discrete single-stage BJT amplifiers. In addition to the remarks already made throughout this section about the characteristics and areas of applicability of the various configurations, we make the following concluding points:

1. The CE configuration is the best suited for realizing the bulk of the gain required in an amplifier. Depending on the magnitude of the gain required, either a single stage or a cascade of two or three stages can be used.
2. Including a resistor $R_e$ in the emitter lead of the CE stage provides a number of performance improvements at the expense of gain reduction.
3. The low input resistance of the CB amplifier makes it useful only in specific applications. As we shall see in Chapter 8, it has a much superior high-frequency response than the CE amplifier. This will make it useful as a high-frequency amplifier, especially when combined with the CE circuit. We shall see one such combination in Chapter 6.
4. The emitter follower finds application as a voltage buffer for connecting a high-resistance source to a low-resistance load and as the output stage in a multistage amplifier.

Finally, we should point out that the Exercises in this section (except for that relating to the emitter follower) used the same component values to allow numerical comparisons.

### TABLE 5.6 Characteristics of Single-Stage Discrete BJT Amplifiers

#### Common Emitter

\[
\begin{align*}
R_u &= R_L \ || (r_e + R_G) \\
\alpha_e &= -\frac{g_m}{r_e + R_G} \\
R_{aux} &= r_e + r_C \\
G_e &= \frac{\beta (r_e + R_G)}{r_e + R_C + R_L} \\
\beta_{aux} &= -\frac{\beta g_m}{r_e + R_G} \\
\end{align*}
\]

#### Common Emitter with Emitter Resistance

Neglecting \( r_e \):

\[
\begin{align*}
R_u &= R_C \ || (1 + \frac{r_e}{r_C + R_L}) \\
\alpha_e &= -\frac{g_m}{r_C + R_L} \\
R_{aux} &= R_C + \frac{r_e}{r_C + R_L} \\
G_e &= \frac{\beta (R_C + R_L)}{R_C + (1 + \frac{r_e}{r_C + R_L})} \\
\beta_{aux} &= -\frac{\beta g_m}{r_C + R_L} \\
\end{align*}
\]
5.8 THE BJT INTERNAL CAPACITANCES AND HIGH-FREQUENCY MODEL

Thus far we have assumed transistor action to be instantaneous, and as a result the transistor models we have developed do not include any elements (i.e., capacitors or inductors) that would cause time or frequency dependence. Actual transistors, however, exhibit charge-storage phenomena that limit the speed and frequency of their operation. We have already encountered such effects in our study of the pn junction in Chapter 3 and learned that they can be modeled as capacitances. In the following we study the charge-storage effects that take place in the BJT and take them into account by adding capacitances to the hybrid-π model.
model. The resulting augmented BJT model will be able to predict the observed dependence of amplifier gain on frequency and the time delays that transistor switches and logic gates exhibit.

5.8.1 The Base-Charging or Diffusion Capacitance $C_{de}$

When the transistor is operating in the active or saturation modes, minority-carrier charge is stored in the base region. In fact, we have already derived an expression for this charge, $Q_n$, in the case of an npn transistor operating in the active mode (Eq. 5.7). Using the result in Eq. (5.7) together with Eqs. (5.3) and (5.4), we can express $Q_n$ in terms of the collector current $i_C$ as

$$Q_n = \frac{W^2}{2D_n} i_C = \tau_F i_C \quad (5.150)$$

where $\tau_F$ is a device constant,

$$\tau_F = \frac{W^2}{2D_n} \quad (5.151)$$

with the dimension of time. It is known as the forward base-transit time and represents the average time a charge carrier (electron) spends in crossing the base. Typically, $\tau_F$ is in the range of 10 ps to 100 ps. For operation in the reverse active mode, a corresponding constant $\tau_R$ applies and is many orders of magnitude larger than $\tau_F$.

Equation (5.151) applies for large signals and, since $i_C$ is exponentially related to $v_{BE}$, $Q_n$ will similarly depend on $v_{BE}$. Thus this charge-storage mechanism represents a nonlinear capacitive effect. However, for small signals we can define the small-signal diffusion capacitance $C_{de}$,

$$C_{de} = \frac{dQ_n}{dv_{BE}} \quad (5.152)$$

resulting in

$$C_{de} = \tau_F \frac{d(i_C)}{dv_{BE}} = \tau_F \frac{V_T}{V_{BE}^0} \quad (5.153)$$

5.8.2 The Base–Emitter Junction Capacitance $C_{je}$

Using the development in Chapter 3, and in particular Eq. (3.X), the base–emitter junction or depletion-layer capacitance $C_{je}$ can be expressed as

$$C_{je} = \frac{C_{je0}}{1 - \frac{V_{BE}}{V_{BE0}}} \quad (5.154)$$

where $C_{je0}$ is the value of $C_{je}$ at zero voltage, $V_{BE0}$ is the EBJ built-in voltage (typically, 0.9 V), and $m$ is the grading coefficient of the EBJ junction (typically, 0.5). It turns out, however, that because the EBJ is forward biased in the active mode, Eq. (5.154) does not provide an accurate prediction of $C_{je}$. Alternatively, one typically uses an approximate value for $C_{je}$,

$$C_{je} \approx 2C_{je0} \quad (5.155)$$
5.8.3 The Collector–Base Junction Capacitance \( C_{\mu} \)

In active-mode operation, the CBJ is reverse biased, and its junction or depletion capacitance, usually denoted \( C_{\mu} \), can be found from

\[
C_{\mu} = \frac{C_{\mu 0}}{\left(1 + \frac{V_c}{V_{0c}}\right)^m}
\]

where \( C_{\mu 0} \) is the value of \( C_{\mu} \) at zero voltage, \( V_{0c} \) is the CBJ built-in voltage (typically, 0.75 V), and \( m \) is its grading coefficient (typically, 0.2–0.5).

5.8.4 The High-Frequency Hybrid-\( \pi \) Model

Figure 5.67 shows the hybrid-\( \pi \) model of the BJT, including capacitive effects. Specifically, there are two capacitances: the emitter–base capacitance \( C_{\pi} = C_{de} + C_{je} \) and the collector–base capacitance \( C_{\mu} \). Typically, \( C_{\pi} \) is in the range of a few picofarads to a few tens of picofarads, and \( C_{\mu} \) is in the range of a fraction of a picofarad to a few picofarads. Note that we have also added a resistor \( r_x \) to model the resistance of the silicon material of the base region between the base terminal \( B \) and a fictitious internal, or intrinsic, base terminal \( B' \) that is right under the emitter region (refer to Fig. 5.6). Typically, \( r_x \) is a few tens of ohms, and its value depends on the current level in a rather complicated manner. Since (usually) \( r_x \ll r_{\pi} \), its effect is negligible at low frequencies. Its presence is felt, however, at high frequencies, as will become apparent later.

The values of the hybrid-\( \pi \) equivalent circuit parameters can be determined at a given bias point using the formulas presented in this chapter. They can also be found from the terminal measurements specified on the BJT data sheets as described in Appendix X. For computer simulation, SPICE uses the parameters of the given IC technology to evaluate the BJT model parameters (Section 5.11).

Before proceeding, a note on notation is in order. Since we are now dealing with voltages and currents that are functions of frequency, we have reverted to using symbols that are uppercase letters with lowercase subscripts (e.g., \( V_\pi, I_\pi \)). This conforms to the notation system used throughout this book.

5.8.5 The Cutoff Frequency

The transistor data sheets do not usually specify the value of \( C_{\pi} \). Rather, the behavior of \( \beta \) or \( h_{fe} \) versus frequency is normally given. In order to determine \( C_{\pi} \) and \( C_{\mu} \) we shall derive an expression for \( h_{fe} \), the CE short-circuit current gain, as a function of frequency in terms of
the hybrid-π components. For this purpose consider the circuit shown in Fig. 5.68, in which the collector is shorted to the emitter. A node equation at C provides the short-circuit collector current $I_c$ as

$$I_c = (g_m - sC_m)V_x$$  \hspace{1cm} (5.157)

A relationship between $V_x$ and $I_b$ can be established by multiplying $I_b$ by the impedance seen between B' and E:

$$V_x = I_b (r_x \parallel C_x \parallel C_m) = \frac{I_b}{\frac{1}{r_x} + sC_x + sC_m}$$  \hspace{1cm} (5.158)

Thus $h_{fe}$ can be obtained by combining Eqs. (5.157) and (5.158):

$$h_{fe} = \frac{I_c}{I_b}$$

Thus, $h_{fe} = \frac{g_m - sC_m}{1 + s(C_x + C_m)\frac{r_x}{s}}$

At the frequencies for which this model is valid, $g_m \gg \omega C_x$; thus we can neglect the $sC_m$ term in the numerator and write

$$h_{fe} = \frac{g_m r_x}{1 + s(C_x + C_m)\frac{r_x}{s}}$$  \hspace{1cm} (5.159)

Thus,

$$h_{fe} = \frac{\beta_0 r_x}{1 + s(C_x + C_m)\frac{r_x}{s}}$$

where $\beta_0$ is the low-frequency value of $\beta$. Thus $h_{fe}$ has a single-pole (or STC) response\(^\ast\) with a 3-dB frequency at $\omega = \omega_T$ where

$$\omega_T = \beta_0 r_x (C_x + C_m)$$  \hspace{1cm} (5.160)

Figure 5.69 shows a Bode plot for $h_{fe}$. From the -6-dB/octave slope it follows that the frequency at which $|h_{fe}|$ drops to unity, which is called the unity-gain bandwidth $\omega_p$, is given by

$$\omega_p = \beta_0 \omega_T$$  \hspace{1cm} (5.161)

\(^\ast\) The frequency response of single-time-constant (STC) networks was reviewed in Section 1.6. A more detailed discussion of this important topic can be found in Appendix X.
Thus,
\[
\omega_T = \frac{\frac{g_m}{C_{\pi}}}{C_{\pi} + C_{\mu}}
\]  
(5.162)
and
\[
f_T = \frac{\frac{\omega_T}{2\pi}}{C_{\pi} + C_{\mu}}
\]  
(5.163)

The unity-gain bandwidth \(f_T\) is usually specified on the data sheets of the transistor. In some cases \(f_T\) is given as a function of \(I_C\) and \(V_{CE}\). To see how \(f_T\) changes with \(I_C\), recall that \(g_m\) is directly proportional to \(I_C\), but only part of \(C_{\pi}\) (the diffusion capacitance \(C_{de}\)) is directly proportional to \(I_C\). It follows that \(f_T\) decreases at low currents, as shown in Fig. 5.70. However, the decrease in \(f_T\) at high currents, also shown in Fig. 5.70, cannot be explained by this argument; rather it is due to the same phenomenon that causes \(h_{fe}\) to decrease at high currents. In the region where \(f_T\) is almost constant, \(C_{\pi}\) is dominated by the diffusion part.

Typically, \(f_T\) is in the range of 100 MHz to tens of GHz. The value of \(f_T\) can be used in Eq. (5.163) to determine \(C_{\pi} + C_{\mu}\). The capacitance \(C_{\mu}\) is usually determined separately by measuring the capacitance between base and collector at the desired reverse-bias voltage \(V_{CB}\).
Before leaving this section, we should mention that the hybrid-π model of Fig. 5.68 characterizes transistor operation fairly accurately up to a frequency of about 0.2 \( f_T \). At higher frequencies one has to add other parasitic elements to the model as well as refine the model to account for the fact that the transistor is in fact a distributed-parameter network that we are trying to model with a lumped-component circuit. One such refinement consists of splitting \( r_x \) into a number of parts and replacing \( C_\pi \) by a number of capacitors, each connected between the collector and one of the taps of \( r_x \). This topic is beyond the scope of this book.

An important observation to make from the high-frequency model of Fig. 5.68 is that at frequencies above 5 to 10 \( f_\beta \), one may ignore the resistance \( r_\pi \). It can be seen then that \( r_x \) becomes the only resistive part of the input impedance at high frequencies. Thus \( r_x \) plays an important role in determining the frequency response of transistor circuits at high frequencies. It follows that an accurate determination of \( r_x \) should be made from a high-frequency measurement.

### EXERCISES

5.48 Find \( C_{de} \), \( C_{je} \), \( C_\pi \), \( C_\mu \), and \( f_T \) for a BJT operating at a dc collector current \( I_C = 1 \) mA and a CBJ reverse bias of 2 V. The device has \( \tau_F = 20 \) ps, \( C_{je0} = 20 \) fF, \( C_\mu_0 = 20 \) fF, \( V_{be0} = 0.9 \) V, \( V_{ce0} = 0.5 \) V, and \( m_{CBJ} = 0.33 \).

**Ans.** 0.8 pF; 40 fF; 0.84 pF; 12 fF; 7.47 GHz

5.49 For a BJT operated at \( I_C = 1 \) mA, determine \( f_T \) and \( C_\pi \) if \( C_\mu = 2 \) pF and \( f_T = 10 \) at 50 MHz.

**Ans.** 500 MHz; 10.7 pF

5.50 If \( C_\pi \) of the BJT in Exercise 5.49 includes a relatively constant depletion-layer capacitance of 2 pF, find \( f_T \) of the BJT when operated at \( I_C = 0.1 \) mA.

**Ans.** 130.7 MHz

### 5.8.6 Summary

For convenient reference, Table 5.7 provides a summary of the relationships used to compose the values of the parameters of the BJT high-frequency model.

#### TABLE 5.7 The BJT High-Frequency Model

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>( g_m )</td>
<td>( I_C/V_T )</td>
</tr>
<tr>
<td>( r_x )</td>
<td>( V_A/I_C )</td>
</tr>
<tr>
<td>( r_s )</td>
<td>( \beta g_m )</td>
</tr>
<tr>
<td>( C_{se} + C_{sj} )</td>
<td>( \frac{C_{be} + C_{p}}{2f_T} )</td>
</tr>
<tr>
<td>( C_A )</td>
<td>( C_{be} + C_{p} )</td>
</tr>
<tr>
<td>( C_{le} )</td>
<td>( r_x g_m )</td>
</tr>
<tr>
<td>( C_{\mu} + 2C_{\mu 0} )</td>
<td>( C_{be} [1 + V_{be0}^m] )</td>
</tr>
<tr>
<td>( m )</td>
<td>( 0.3–0.5 )</td>
</tr>
</tbody>
</table>
5.9 FREQUENCY RESPONSE OF THE COMMON-EMITTER AMPLIFIER

In this section we study the dependence of the gain of the BJT common-emitter amplifier of Fig. 5.71(a) on the frequency of the input signal.

5.9.1 The Three Frequency Bands

When the common-emitter amplifier circuit of Fig. 5.71(a) was studied in Section 5.7.3, it was assumed that the coupling capacitors $C_1$ and $C_2$ and the bypass capacitor $C_e$ were

![Diagram of the common-emitter amplifier circuit](image)

**FIGURE 5.71** (a) Capacitively coupled common-emitter amplifier. (b) Sketch of the magnitude of the gain of the CE amplifier versus frequency. The graph delineates the three frequency bands relevant to frequency response determination.
acting as perfect short circuits at all signal frequencies of interest. We also neglected the internal capacitances of the BJT. That is, $C_C$ and $C_E$ of the BJT high-frequency model (Fig. 5.67) were assumed to be sufficiently small to act as open circuits at all signal frequencies of interest. As a result of ignoring all capacitive effects, the gain expressions derived in Section 5.7.3 were independent of frequency. In reality, however, this situation only applies over a limited, though usually wide, band of frequencies. This is illustrated in Fig. 5.71(b), which shows a sketch of the magnitude of the overall voltage gain, $|G_v|$, of the common-emitter amplifier versus frequency. We observe that the gain is almost constant over a wide frequency band, called the midband. The value of the midband gain $A_{M}$ corresponds to the overall voltage gain $G_v$ that we derived in Section 5.7.3, namely,

$$A_{M} = \frac{V_o}{V_{sig}} = -\frac{R_G V_{CE}}{R_E + R_C (R_L / R_E)} \quad (5.164)$$

Figure 5.71(b) shows that the gain falls off at signal frequencies below and above the midband. The gain falloff in the low-frequency band is due to the fact that even though $C_C$, $C_C$, and $C_E$ are large capacitors (typically, in the µF range), as the signal frequency is reduced their impedances increase and they no longer behave as short circuits. On the other hand, the gain falls off in the high-frequency band as a result of $C_{gs}$ and $C_{gd}$, which though very small (in the fraction of a pF to the pF range), their impedances at sufficiently high frequencies decrease; thus they can no longer be considered as open circuits. Our objective in this section is to study the mechanisms by which these two sets of capacitances affect the amplifier gain in the low-frequency and the high-frequency bands. In this way we will be able to determine the frequencies $f_L$ and $f_H$, which define the extent of the midband, as shown in Fig. 5.71(b).

The midband is obviously the useful frequency band of the amplifier. Usually, $f_L$ and $f_H$ are the frequencies at which the gain drops by 3 dB below its value at midband; that is, at $f_L$ and $f_H$, $|G_v| = |A_{M}|/(\sqrt{2})$. The amplifier bandwidth or 3-dB bandwidth is defined as the difference between the lower ($f_L$) and upper or higher ($f_H$) 3-dB frequencies:

$$BW = f_H - f_L \quad (5.165)$$

Since usually $f_L \ll f_H$

$$BW = f_H$$

A figure-of-merit for the amplifier is its gain–bandwidth product, defined as

$$GB = |A_{M}|BW \quad (5.166)$$

It will be shown at a later stage that in amplifier design, it is usually possible to trade-off gain for bandwidth. One way of accomplishing this, for instance, is by including an emitter-degeneration resistance $R_e$, as we have done in Section 5.7.4.

### 5.9.2 The High-Frequency Response

To determine the gain, or the transfer function, of the amplifier of Fig. 5.71(a) at high frequencies, and in particular the upper 3-dB frequency $f_H$, we replace the BJT with its high-frequency model of Fig. 5.67. At these frequencies $C_C$, $C_C$, and $C_E$ will be behaving as perfect short circuits. The result is the high-frequency amplifier equivalent circuit shown in Fig. 5.72(a).
The equivalent circuit of Fig. 5.72(a) can be simplified by utilizing Thévenin theorem at the input side and by combining the three parallel resistances at the output side. Specifically, the reader should be able to show that applying Thévenin theorem twice simplifies the resistive network at the input side to a signal generator $V'_{in}$ and a resistance $R'_{in}$.

\[
V'_{in} = \frac{R_2}{R_2 + R_{in}} \left( r_e + r_s + (R_{in} | R_b) \right)
\]

\[
R'_{in} = r_e (R_c | R_b)
\]

\[
V'_{out} = V_c + \frac{r_e}{R_c + R_{in}} \left( r_e + r_s + (R_{in} | R_b) \right)
\]

\[
R'_{out} = r_e (R_c | R_b)
\]

**Figure 5.72** Determining the high-frequency response of the CE amplifier: (a) equivalent circuit; (b) the circuit of (a) simplified at both the input side and the output side; (c) equivalent circuit with $C_a$ replaced at the input side with the equivalent capacitance $C_{eq}$. 
where

\[ V_{oq} = V_{eq} \frac{R_b}{R_b + R_{eq} + \frac{r_x}{r_x + (R_m \parallel R_b)}} \]  \hspace{1cm} (5.167)

\[ R_{eq} = r_e \parallel [r_x + (R_b \parallel R_m)] \]  \hspace{1cm} (5.168)

Observe that \( R_{eq} \) is the resistance seen looking back into the resistive network between nodes \( B' \) and \( E \).

The circuit in Fig. 5.72(b) can be simplified further if we can find a way to deal with the bridging capacitance \( C_\mu \) that connects the output node to the “input” node, \( B' \). Toward that end consider first the output node. It can be seen that the load current is \( (g_m V_\pi - I_\mu) \), where \( g_m V_\pi \) is the output current of the transistor and \( I_\mu \) is the current supplied through the very small capacitance \( C_\mu \). In the vicinity of \( f_H \), which is close to the edge of the midband, it is reasonable to assume that \( I_\mu \) is still much smaller than \( g_m V_\pi \), with the result that \( V_o \) can be given approximately by

\[ V_o \approx g_m V_\pi RL \]  \hspace{1cm} (5.169)

Since \( V_o = V_{eq} \), Eq. (5.169) indicates that the gain from \( B' \) to \( C \) is \(-g_m R_L'\), the same value as in the midband. The current \( I_\mu \) can now be found from

\[ I_\mu = sC_\mu (V_o - V_x) \]

\[ = sC_\mu [(V_o - (g_m R_L' V_x))] \]

\[ = sC_\mu (1 + g_m R_L') V_x \]

Now, in Fig. 5.72(b), the left-hand-side of the circuit, at XX', knows of the existence of \( C_\mu \) only through the current \( I_\mu \). Therefore we can replace \( C_\mu \) by an equivalent capacitance \( C_{eq} \) between \( B' \) and ground as long as \( C_{eq} \) draws a current equal to \( I_\mu \) that is,

\[ sC_{eq} V_x = I_\mu = sC_\mu (1 + g_m R_L') V_x \]
5.9 FREQUENCY RESPONSE OF THE COMMON-EMITTER AMPLIFIER

which results in

\[ C_{eq} = C_s(1 + g_m R'_L) \]  

(5.170)

Using \( C_{eq} \) enables us to simplify the equivalent circuit at the input side to that shown in Fig. 5.72(c), which we recognize as a single-time-constant (STC) network of the low-pass type (see Section 1.6 and Appendix X). Therefore we can express \( V_x \) in terms of as

\[ V_x = V'_x \frac{1}{1 + s/\omega_0} \]  

(5.171)

where \( \omega_0 \) is the corner frequency of the STC network composed of \( C_{in} \) and \( R'_L \).

\[ \omega_0 = \frac{1}{C_{eq} R'_L} \]  

(5.172)

where \( C_{eq} \) is the total input capacitance at \( B' \).

\[ C_{in} = C_x + C_{eq} = C_s + C_x(1 + g_m R'_L) \]  

(5.173)

and \( R'_L \) is the effective source resistance, given by Eq. (5.168). Combining Eqs. (5.169), (5.171), and (5.167) give the voltage gain in the high-frequency band as

\[ \frac{V_{th}}{V_{eq}} = \frac{A_{th} R'_L}{1 + s/\omega_0} \]  

(5.174)

The quantity between the square brackets of Eq. (5.174) is the midband gain, and except for the fact that here \( r_s \) is taken into account, this expression is the same as that in Eq. (5.164). Thus,

\[ \frac{V_x}{V_{eq}} = \frac{A_{th} R'_L}{1 + s/\omega_0} \]  

(5.175)

from which we deduce that the upper 3-dB frequency \( f_H \) must be

\[ f_H = \frac{\omega_0}{2\pi} = \frac{1}{2\pi C_{in} R'_L} \]  

(5.176)

We thus see that the high-frequency response will be that of a low-pass STC network with a 3-dB frequency \( f_H \) determined by the time constant \( C_{eq} R'_L \). Fig. 5.72(d) shows a sketch of the magnitude of the high-frequency gain.

Before leaving this section we wish to make a number of observations:

1. The upper 3-dB frequency is determined by the interaction of \( R'_L \) and \( C_{in} \). If \( R_L \gg R_{eq} \) and \( r_s \ll R_{eq} \), then \( R'_{eq} \approx R'_L \parallel r_s \). Thus the extent to which \( R_{eq} \) determines \( f_H \) depends on its value relative to \( r_s \). If \( R_{eq} \gg r_s \), then \( R'_{eq} \approx r_s \), on the other hand, if \( R_{eq} \) is on the order of or smaller than \( r_s \), then it has much greater influence on the value of \( f_H \).

2. The input capacitance \( C_{in} \) is usually dominated by \( C_{eq} \), which in turn is made large by the multiplication effect that \( C_x \) undergoes. Thus, although \( C_x \) is usually very small, its effect on the amplifier frequency response can be significant as a result of its
multiplication by the factor \((1 + g_m R'_L)\), which is approximately equal to the midband gain of the amplifier.

3. The multiplication effect that \(C_a\) undergoes comes about because it is connected between two nodes (B' and C) whose voltages are related by a large negative gain \((-g_m R'_L)\). This effect is known as the Miller effect, and \((1 + g_m R'_L)\) is known as the Miller multiplier. It is the Miller effect that causes the CE amplifier to have a large input capacitance \(C_a\) and hence a low \(f_H\).

4. To extend the high-frequency response of a BJT amplifier, we have to find configurations in which the Miller effect is absent or at least reduced. We shall return to this subject at great length in Chapter 8.

5. The above analysis, resulting in an STC or a single-pole response, is a simplified one. Specifically, it is based on neglecting \(I_{\mu}\) relative to \(g_m V_\pi\), an assumption that applies well at frequencies not too much higher than \(f_H\). A more exact analysis of the circuit in Fig. 5.72(a) will be considered in Chapter 8. The results above, however, are more than sufficient for our current needs.

**EXAMPLE 5.18**

It is required to find the midband gain and the upper 3-dB frequency of the common-emitter amplifier of Fig. 5.71(a) for the following case:

\[ V_{CC} = V_{EE} = 10 \text{ V}, \quad I = 1 \text{ mA}, \quad R_B = 100 \text{ k}\Omega, \quad R_C = 8 \text{ k}\Omega, \quad R_{\text{sig}} = 5 \text{ k}\Omega, \quad R_L = 5 \text{ k}\Omega, \quad V_T = 100 \text{ V}, \quad C_\mu = 1 \text{ pF}, \quad f_T = 800 \text{ MHz}, \text{ and } r_x = 50 \text{ } \Omega. \]

**Solution**

The transistor is biased at \(I_C \approx 1 \text{ mA}. \) Thus the values of its hybrid-\(\pi\) model parameters are

\[
\begin{align*}
g_m &= \frac{I_C}{V_T} = \frac{1 \text{ mA}}{25 \text{ mV}} = 40 \text{ mA/V} \\
r_p &= \frac{R_B}{g_m} = \frac{100 \text{ k}\Omega}{40 \text{ mA/V}} = 2.5 \text{ k}\Omega \\
r_e &= \frac{V_A}{I_C} = \frac{100 \text{ V}}{1 \text{ mA}} = 100 \text{ k}\Omega \\
C_x + C_p &= \frac{g_m}{2\pi f_T} = \frac{40 \times 10^{-3}}{2\pi \times 800 \times 10^6} = 8 \text{ pF} \\
C_e &= 1 \text{ pF} \\
C_y &= 7 \text{ pF} \\
r_\pi &= 50 \text{ } \Omega
\end{align*}
\]

The midband voltage gain is

\[
A_{HV} = -\frac{R_E}{R_B + R_E} \frac{r_x}{r_x + (R_E \parallel R_{\text{sig}})R_L'}
\]

where

\[
R_L' = r_x \parallel R_C \parallel R_L = (100 \parallel 8 \parallel 5) \text{ k}\Omega = 3 \text{ k}\Omega
\]
Thus,

\[ g_m R'_L = 40 \times 3 = 120 \text{ V/V} \]

and

\[ A_H = \frac{100}{100 + 5} \times \frac{2.5}{2.5 + 0.05 + \{100\|5\}} \times 120 \]

\[ = -39 \text{ V/V} \]

and

\[ 20 \log |A_H| = 32 \text{ dB} \]

To determine \( f_H \) we first find \( C_{in} \)

\[ C_{in} = C_c + C_b (1 + g_m R'_L) \]

\[ = 7 + (1 + 120) = 128 \text{ pF} \]

and the effective source resistance \( R'_{se} \)

\[ R'_{se} = r_s \| (r_h \| R_{in}) \]

\[ = 2.5 \| (0.05 + (100 \| 5)) \]

\[ = 1.65 \text{ k}\Omega \]

Thus,

\[ f_H = \frac{1}{2 \pi C_{in} R'_{se}} = \frac{1}{2 \pi \times 128 \times 10^{-12} \times 1.65 \times 10^3} = 754 \text{ kHz} \]

EXERCISE

5.51 For the amplifier in Example 5.18, find the value of \( R_L \) that reduces the midband gain to half the value found. What value of \( f_H \) results? Note the trade-off between gain and bandwidth.

Ans. 1.9 k\Omega; 1.42 MHz

5.9.3 The Low-Frequency Response

To determine the low-frequency gain or transfer function of the common-emitter amplifier circuit, we show in Fig. 5.73(a) the circuit with the dc sources eliminated (current source \( I \) open circuited and voltage source \( V_{CC} \) short circuited). We shall perform the small-signal analysis directly on this circuit. We will, of course, ignore \( C_c \) and \( C_b \) since at such low frequencies their impedances will be very high and thus can be considered as open circuits. Also, to keep the analysis simple and thus focus attention on the mechanisms that limit the amplifier gain at low frequencies, we will neglect \( r_s \). The reader can verify through SPICE simulation that the effect of \( r_s \) on the low-frequency amplifier gain is small. Finally, we shall also neglect \( r_h \), which is usually much smaller than \( r_n \), with which it appears in series.
FIGURE 5.73 Analysis of the low-frequency response of the CE amplifier: (a) amplifier circuits with dc sources removed; (b) the effect of $C_{g1}$ is determined with $C_E$ and $C_{g2}$ assumed to be acting as perfect short circuits; (c) the effect of $C_E$ is determined with $C_{g1}$ and $C_{g2}$ assumed to be acting as perfect short circuits.

\[ f_{P1} = \frac{1}{2 \pi} C_{g1} \left( \frac{R_B}{r_e} + R_S \right) \]

\[ f_{P2} = \frac{1}{2 \pi} C_E \left( r_e + \frac{R_S R_B}{\beta + 1} \right) \]
5.9 FREQUENCY RESPONSE OF THE COMMON-EMITTER AMPLIFIER

Our first cut at the analysis of the circuit in Fig. 5.72(a) is to consider the effect of the three capacitors $C_C$, $C_E$, and $C_C$ one at a time. That is, when finding the effect of $C_C$, we shall assume that $C_E$ and $C_C$ are acting as perfect short circuits, and when considering $C_E$, we assume that $C_C$ and $C_C$ are perfect short circuits, and so on. This is obviously a major simplifying assumption—and one that might not be justified. However, it should serve as a first cut at the analysis enabling us to gain insight into the effect of these capacitances.

Figure 5.72(b) shows the circuit with $C_C$ and $C_C$ replaced with short circuits. The voltage $V_\pi$ at the base of the transistor can be written as

$$V_\pi = \frac{V_{in}}{(R_b \parallel r_b) + R_{in} + \frac{1}{sC_C}}$$

and the output voltage is obtained as

$$V_o = -g_m V_\pi (R_C \parallel R_L)$$

FIGURE 5.73 (Continued) (d) the effect of $C_C$ is determined with $C_C$ and $C_C$ assumed to be acting as perfect short circuits; (e) sketch of the low-frequency gain under the assumptions that $C_C$, $C_E$, and $C_C$ do not interact and that their break (or pole) frequencies are widely separated.
These two equations can be combined to obtain the voltage gain \( \frac{V_o}{V_{in}} \) including the effect of \( C_C \) as

\[
\frac{V_o}{V_{in}} = \frac{(R_B \parallel R_C) \parallel R_C}{(R_B \parallel r_1) + R_C} \left( \frac{s}{C_C (R_B \parallel r_1) + R_C} \right) \tag{5.177}
\]

from which we observe that the effect of \( C_C \) is to introduce the frequency-dependent factor between the square brackets on the right-hand side of Eq. (5.177). We recognize this factor as the transfer fraction of a single-time-constant (STC) network of the high-pass type (see Section 1.6 and Appendix X) with a corner or break frequency \( \omega_P \).

\[
\omega_P = \frac{1}{C_C (R_B \parallel r_1) + R_C} \tag{5.178}
\]

Note that is the resistance seen between the terminals of \( C_C \) when \( V_{sig} \) is set to zero. The STC high-pass factor introduced by \( C_C \) will cause the amplifier gain to roll off at low frequencies at the rate of 6 dB/octave (20 dB/decade) with a 3-dB frequency at

\[
f_P = \frac{1}{2 \pi \omega_P} \tag{5.179}
\]

Next, we consider the effect of \( C_E \). For this purpose we assume that \( C_C \) and \( C_C \) are acting as perfect short circuits and thus obtain the circuit in Fig. 5.73(c). Reflecting \( re \) and \( CE \) into the base circuit and utilizing the Thévenin theorem enables us to obtain the base current as

\[
I_b = \frac{V_{in} R_C}{R_B + R_{C1} (R_C \parallel R_{Cn}) + (\beta + 1)(r_1 + \frac{1}{C_E})} \tag{5.180}
\]

The collector current can then be found as \( \beta I_b \) and the output voltage as

\[
V_o = -\beta \left( R_C \parallel R_C \right) \left( \frac{1}{R_B + R_{C1} (R_C \parallel R_{Cn}) + (\beta + 1)(r_1 + \frac{1}{C_E})} \right) V_{in} \tag{5.181}
\]

Thus the voltage gain including the effect of \( C_E \) can be expressed as

\[
\frac{V_o}{V_{in}} = \frac{R_C}{R_B + R_{C1} (R_C \parallel R_{Cn}) + (\beta + 1)(r_1 + \frac{1}{C_E})} \left( \frac{s}{1/C_E (r_1 + \frac{1}{C_E}) + \beta + 1} \right) \tag{5.182}
\]

We observe that \( C_E \) introduces the STC high-pass factor on the extreme right-hand side. Thus \( C_E \) causes the gain to fall off at low frequencies at the rate of 6 dB/octave with a 3-dB frequency equal to the corner or break frequency of the high-pass STC factor; that is,

\[
\omega_P = \frac{1}{C_E (r_1 + \frac{1}{C_E}) + \beta + 1} \tag{5.183}
\]

Observe that \( (r_1 + (R_C \parallel R_{Cn})/(\beta + 1)) \) is the resistance seen between the two terminals of \( C_C \) when \( V_{in} \) is set to zero. The effect of \( C_E \) on the amplifier frequency response is illustrated by the sketch in Fig. 5.73(c).
Finally, we consider the effect of $C_{C2}$. The circuit with $C_{C1}$ and $C_E$ assumed to be acting as perfect short circuits is shown in Fig. 5.73(d), for which we can write

$$V_e = V_{in} \frac{R_B}{(R_B || r_e) + R_{in}}$$

and

$$V_{in} = -g_m V_{o} \frac{R_C}{R_C + \frac{1}{C_{C2}} + R_L}$$

These two equations can be combined to obtain the low-frequency gain including the effect of $C_{C2}$ as

$$\frac{V_o}{V_{in}} = -g_m V_{o} \frac{R_C}{R_C + \frac{1}{C_{C2}} + R_L} \left[ \frac{s}{s + \frac{1}{C_{C2}(R_C + R_L)}} \right]$$  \hspace{1cm} (5.181)

We observe that $C_{C2}$ introduces the frequency-dependent factor between the square brackets, which we recognize as the transfer function of a high-pass STC network with a break frequency $\omega_{P3}$

$$\omega_{P3} = \frac{1}{C_{C2}(R_C + R_L)}$$  \hspace{1cm} (5.182)

Here we note that as expected, $(R_C + R_L)$ is the resistance seen between the terminals of $C_{C2}$ when $V_{in}$ is set to zero. Thus capacitor $C_{C2}$ causes the low-frequency gain of the amplifier to decrease at the rate of 6 dB/octave with a 3-dB frequency at $f_{P3} = \omega_{P3}/2\pi$, as illustrated by the sketch in Fig. 5.73(d).

Now that we have determined the effects of $C_{C1}$ and of $C_{C2}$ acting alone, the question becomes what will happen when all three are present at the same time. This question has two parts: First, what happens when all three capacitors are present but do not interact? The answer is that the amplifier low-frequency gain can be expressed as

$$\frac{V_o}{V_{in}} = -A_d \left( \frac{s}{s + \omega_{P1}} \right) \left( \frac{s}{s + \omega_{P2}} \right) \left( \frac{s}{s + \omega_{P3}} \right)$$  \hspace{1cm} (5.183)

from which we see that it acquires three break frequencies at $f_{P1}, f_{P2},$ and $f_{P3}$ all in the low-frequency band. If the three frequencies are widely separated, their effects will be distinct, as indicated by the sketch in Fig. 5.73(e). The important point to note here is that the 3-dB frequency $f_{P3}$ is determined by the highest of the three break frequencies. This is usually the break frequency caused by the bypass capacitor $C_E$, simply because the resistance that it sees is usually quite small. Thus, even if one uses a large value for $C_E, f_{P3}$ is usually the highest of the three break frequencies.

If $f_{P1}, f_{P2},$ and $f_{P3}$ are close together, none of the three dominates, and to determine $f_{P}$ we have to evaluate $|V_o/V_{in}|$ in Eq. (5.183) and calculate the frequency at which it drops to $|A_d|/\sqrt{2}$. The work involved in doing this, however, is usually too great and is rarely justified in practice, particularly because in any case, Eq. (5.183) is an approximation based on the assumption that the three capacitors do not interact. This leads to the second part of the question: What happens when all three capacitors are present and interact? We do know that $C_{C1}$ and $C_E$ usually interact and that their combined effect is two poles at frequencies that will differ from $\omega_{P1}$ and $\omega_{P2}$. Of course, one can derive the overall transfer function taking this interaction into account and find more precisely the low-frequency response. This, however, will be too complicated to yield additional insight. As an alternative, for hand...
calculations we can obtain a reasonably good estimate for $f_L$ using the following formula (which we will not derive here):

$$f_L = \frac{1}{2\pi \left( \frac{1}{C_1 R_1} + \frac{1}{C_2 R_2} + \frac{1}{C_E R_E} \right)}$$  \hspace{1cm} (5.184)

or equivalently,

$$f_L = f_{T1} + f_{T2} + f_{T3}$$  \hspace{1cm} (5.185)

where $R_1$, $R_2$, and $R_E$ are the resistances seen by $C_1$, $C_2$, and $C_E$, respectively, when $V_{sig}$ is set to zero. Equations (5.184) and (5.185) provide insight regarding the relative contributions of the three capacitors to $f_L$. Finally, we note that a far more precise determination of the low-frequency gain and the 3-dB frequency $f_L$ can be obtained using SPICE (Section 5.11).

Selecting Values for $C_1$, $C_2$, and $C_E$ We now address the design issue of selecting appropriate values for $C_1$, $C_2$, and $C_E$. The design objective is to place the lower 3-dB frequency $f_L$ at a specified location while minimizing the capacitor values. Since as mentioned above $C_E$ usually sees the lowest of the three resistances, the total capacitance is minimized by selecting $C_E$ so that its contribution to $f_L$ is dominant. That is, by reference to Eq. (5.184), we may select $C_E$ such that $1/(C_E R_E)$ is, say, 80% of $\omega_L = 2\pi f_L$, leaving each of the other capacitors to contribute 10% to the value of $\omega_L$. Example 5.19 should help to illustrate this process.

### Example 5.19

We wish to select appropriate values for $C_1$, $C_2$, and $C_E$ for the common-emitter amplifier whose high-frequency response was analyzed in Example 5.18. The amplifier has $R_B = 100 \, k\Omega$, $R_C = 8 \, k\Omega$, $R_L = 5 \, k\Omega$, $R_{sig} = 5 \, k\Omega$, $\beta_0 = 100$, $g_m = 40 \, mA/V$, and $r_\pi = 2.5 \, k\Omega$. It is required to have $f_L = 100 \, Hz$.

**Solution**

We first determine the resistances seen by the three capacitors $C_1$, $C_2$, and $C_E$ as follows:

$$R_{C1} = (R_B \parallel R_{sig}) + R_{3e} = (100 \, k\Omega \parallel 5 \, k\Omega) + 5 = 7.44 \, k\Omega$$

$$R_C = r_\pi + \frac{R_B \parallel R_{sig}}{\beta_0 + 1} = 0.025 + \frac{100 \, k\Omega}{101} = 0.072 \, k\Omega = 72 \, \Omega$$

$$R_{C2} = R_C + R_L = 8 \, k\Omega + 13 \, k\Omega = 13 \, k\Omega$$

Now, selecting $C_E$ so that it contributes 80% of the value of $\omega_L$ gives

$$\frac{1}{C_E \times 72} = 0.8 \times \frac{2 \pi \times 100}{72}$$

$$C_E = 27.6 \, \mu F$$

1 The interested reader can refer to Chapter 7 of the fourth edition of this book.
Next, if \( C_{C1} \) is to contribute 10% of \( f_L \),
\[
\frac{1}{C_{C1} \times 7.44 \times 10^3} = 0.1 \times 2\pi \times 100
\]
\[C_{C1} = 2.1 \mu F\]

Similarly, if \( C_{C2} \) is to contribute 10% of \( f_L \), its value should be selected as follows:
\[
\frac{1}{C_{C2} \times 13 \times 10^3} = 0.1 \times 2\pi \times 100
\]
\[C_{C2} = 1.2 \mu F\]

In practice, we would select the nearest standard values for the three capacitors while ensuring that \( f_L \geq 100 \) Hz.

**EXERCISE**

5.52 A common-emitter amplifier has \( C_{C1} = C_{C2} = 1 \mu F, R_B = 100 \, k\Omega, R_g = 5 \, k\Omega, R_e = 40 \, mA/V, r_e = 2.5 \, k\Omega, R_e = 8 \, k\Omega, \) and \( R_1 = 5 \, k\Omega \). Assuming that the three capacitors do not interact, find \( f_{P1}, f_{P2}, \) and \( f_{P3} \) and hence estimate \( f_L \).

Anw. 21.4 Hz; 2.21 kHz; 12.2 Hz; since \( f_{P2} \approx f_{P3} \) and \( f_{P1} \approx f_{P2} = 2.21 \) kHz, using Eq. (5.185), a somewhat better estimate for \( f_L \) is 2.24 kHz.

5.9.4 A Final Remark

The frequency response of the other amplifier configurations will be studied in Chapter 8.

5.10 THE BASIC BJT DIGITAL LOGIC INVERTER

The most fundamental component of a digital system is the logic inverter. In Section 1.7, the inverter was studied at a conceptual level, and the realization of the inverter using voltage-controlled switches was presented. Having studied the BJT, we can now consider its application in the realization of a simple logic inverter. Such a circuit is shown in Fig. 5.74. The reader will note that we have already studied this circuit in some detail. In fact, we used it in...
Section 5.3.4 to illustrate the operation of the BJT as a switch. The operation of the circuit as a logic inverter makes use of the cutoff and saturation modes. In very simple terms, if the input voltage \( v_I \) is “high,” at a value close to the power-supply voltage \( V_{CC} \), representing a logic 1 in a positive-logic system, the transistor will be conducting and, with appropriate choice of values for \( R_B \) and \( R_C \), saturated. Thus the output voltage will be \( V_{CE(sat)} \approx 0.2 \text{ V} \), representing a “low” or logic 0. Conversely, if the input voltage is “low,” at a value close to ground (e.g., \( V_{CE(sat)} \)), then the transistor will be cut off, \( i_C \) will be zero, and \( v_O = V_{CC} \), which is “high” or logic 1.

The choice of cutoff and saturation as the two modes of operation of the BJT in this inverter circuit is motivated by the following two factors:

1. The power dissipation in the circuit is relatively low in both cutoff and saturation: In cutoff all currents are zero (except for very small leakage currents), and in saturation the voltage across the transistor is very small (\( V_{CE(sat)} \)).
2. The output voltage levels (\( V_{CC} \) and \( V_{CE(sat)} \)) are well defined. In contrast, if the transistor is operated in the active region, \( v_O = V_{CC} - i_C R_C = V_{CC} - \beta i_B R_C \), which is highly dependent on the rather ill-controlled transistor parameter \( \beta \).

5.10.1 The Voltage Transfer Characteristic

As mentioned in Section 1.7, the most useful characterization of an inverter circuit is in terms of its voltage transfer characteristic, \( v_O \) versus \( v_I \). A sketch of the voltage transfer characteristic (VTC) of the inverter circuit of Fig. 5.74 is presented in Fig. 5.75. The transfer characteristic is approximated by three straight-line segments corresponding to the operation of the BJT in the cutoff, active, and saturation regions, as indicated. The actual transfer characteristic will obviously be a smooth curve but will closely follow the straight-line asymptotes indicated. We shall now compute the coordinates of the breakpoints of the transfer

![Figure 5.75](image-url)  
**Figure 5.75** Sketch of the voltage transfer characteristic of the inverter circuit of Fig. 5.74 for the case \( R_B = 10 \text{ k} \Omega, R_C = 1 \text{ k} \Omega, \beta = 50 \), and \( V_{CC} = 5 \text{ V} \). For the calculation of the coordinates of \( X \) and \( Y \), refer to the text.
5.10 THE BASIC BJT DIGITAL LOGIC INVERTER

characteristic of Fig. 5.75 for a representative case—\( R_B = 10 \, \text{k} \Omega, R_C = 1 \, \text{k} \Omega, \beta = 50, \) and \( V_{CC} = 5 \, \text{V} \)—as follows:

1. At \( V_{IL} = V_{CB} = 0.2 \, \text{V}, \) \( V_{O} = V_{OH} = V_{CC} = 5 \, \text{V}. \)

2. At \( V_I = V_{CE}, \) the transistor begins to turn on; thus, \( V_{th} \approx 0.7 \, \text{V}. \)

3. For \( V_{IL} < V_I < V_{IH}, \) the transistor is in the active region. It operates as an amplifier whose small-signal gain is

\[
A_v = \frac{v_o}{v_i} = -\beta \frac{R_C}{R_B + r_e}
\]

The gain depends on the value of \( r_e, \) which in turn is determined by the collector current and hence by the value of \( v_I. \) As the current through the transistor increases, \( r_e \) decreases and we can neglect \( r_e \) relative to \( R_B, \) thus simplifying the gain expression to

\[
A_v = -\beta \frac{R_C}{R_B} = -50 \times \frac{1}{10} = -5 \, \text{V/V}
\]

4. At \( V_I = V_{IB}, \) the transistor enters the saturation region. Thus \( V_{IH} \) is the value of \( v_I \) that results in the transistor being at the edge of saturation,

\[
I_B = \frac{(V_{CC} - V_{CB})}{\beta}
\]

For the values we are using, we obtain \( I_B = 0.096 \, \text{mA}, \) which can be used to find \( V_{IH}. \)

\[
V_{IH} = I_B R_B + V_{BE} = 1.66 \, \text{V}
\]

5. For \( v_I = V_{IH} = 5 \, \text{V}, \) the transistor will be deep into saturation with \( v_{CE} = V_{CE} = 0.2 \, \text{V}, \) and

\[
\beta_{meas} = \frac{(V_{CC} - V_{CE})/R_C}{(V_{IH} - V_{BE})/R_B} = \frac{4.8}{0.43} = 11
\]

6. The noise margins can now be computed using the formulas from Section 1.7,

\[
\text{NM}_H = V_{OH} - V_{IH} = 5 - 1.66 = 3.34 \, \text{V}
\]

\[
\text{NM}_L = V_{IL} - V_{OH} = 0.7 - 0.2 = 0.5 \, \text{V}
\]

Obviously, the two noise margins are vastly different, making this inverter circuit less than ideal.

7. The gain in the transition region can be computed from the coordinates of the breakpoints \( X \) and \( Y. \)

\[
\text{Voltage gain} = \frac{5 - 0.2}{1.66 - 0.7} = -5 \, \text{V/V}
\]

which is equal to the approximate value found above (the fact that it is exactly the same value is a coincidence).

5.10.2 Saturated Versus Nonsaturated BJT Digital Circuits

The inverter circuit just discussed belongs to the saturated variety of BJT digital circuits. A historically significant family of saturated BJT logic circuits is transistor-transistor logic.
Although some versions of TTL remains in use, saturated bipolar digital circuits generally are no longer the technology of choice in digital system design. This is because their speed of operation is severely limited by the relatively long time delay required to turn off a saturated transistor, as we will now explain briefly.

In our study of BJT saturation in Section 5.1.5, we made use of the minority-carrier distribution in the base region (see Fig. 5.10). Such a distribution is shown in Fig. 5.76, where the minority carrier charge stored in the base has been divided into two components: The component represented by the blue triangle produces the gradient that gives rise to the diffusion current across the base; the other component, represented by the gray rectangle, causes the transistor to be driven deeper into saturation. The deeper the transistor is driven into saturation (i.e., the greater the base overdrive factor is), the greater the amount of the “gray” component of the stored charge will be. It is this “extra” stored base charge that represents a serious problem when it comes to turning off the transistor. Before the collector current can begin to decrease, all of the extra stored charge must first be removed. This adds a relatively large component to the turn-off time of a saturated transistor.

From the above we conclude that to achieve high operating speeds, the BJT should not be allowed to saturate. This is the case in current-mode logic and its particular form, emitter-coupled logic (ECL), which will be studied briefly in Chapter 12. There we will show that ECL is currently the highest-speed logic-circuit family available. It is based on the current-switching arrangement that was discussed conceptually in Section 1.7 (Fig. 1.33).

**EXERCISE 5.53** Consider the inverter of Fig. 5.74 when \( v_I \) is low. Let the output be connected to the input terminals of \( N \) identical inverters. Convince yourself that the output level \( V_{OH} \) can be determined using the equivalent circuit shown in Fig. E5.53. Hence show that

\[
V_{OH} = V_{CC} - R_e \frac{V_{CE} - V_{BE}}{R_c + R_e/N}
\]
For $N = 5$, calculate $V_{OH}$ using the component values of the example circuit discussed earlier (i.e., $R_B = 10 \, \text{k}\Omega$, $R_C = 1 \, \text{k}\Omega$, $V_{CC} = 5 \, \text{V}$).

Ans. $3.6 \, \text{V}$

**FIGURE E5.53**
SUMMARY

- Depending on the bias conditions on its two junctions, the BJT can operate in one of four possible modes: cutoff (both junctions reverse biased), active (the EBI forward biased and the CBI reverse biased), saturation (both junctions forward biased), and reverse-active (the EBI reverse biased and the CBI forward biased).

- For amplifier applications, the BJT is operated in the active mode. Switching applications make use of the cutoff and saturation modes. The reverse-active mode of operation is of conceptual interest only.

- A BJT operating in the active mode provides a collector current \( i_C = I_B \beta \frac{V_C}{V_T} \). The base current \( i_B \) and the emitter current \( i_E \) are related by \( i_E = i_C + i_B \). Also, \( i_E = \alpha i_C \), and thus \( \beta = \frac{\alpha}{(1 - \alpha)} \) and \( \alpha = \beta(\beta + 1) \). See Table 5.2.

- The input resistance of the common-emitter amplifier can be increased by including an unbypassed resistance in the emitter lead. This emitter-degeneration resistance provides other performance improvements at the expense of reduced voltage gain.

- For small signals, the BJT functions as a linear voltage-controlled current source with a transconductance \( g_m = \frac{I_C}{V_T} \). The input resistance between base and emitter, the input resistance between base and collector, and the input resistance between collector and emitter are given in Eqs. (5.26) to (5.29).

- For a summary of the characteristics of discrete single-stage amplifier circuits, refer to Table 5.6.

- To operate as a linear amplifier, the BJT is biased in the active region and the signal \( v_{SE} \) is kept small \( (v_{BC} \ll V_T) \).

- For small signals, the BJT functions as a linear voltage-controlled current source with a transconductance \( g_m = \frac{I_C}{V_T} \). The input resistance between base and emitter, looking into the base, is \( r_i = \frac{1}{g_m} \). Simplified low-frequency equivalent-circuit models for the BJT are shown in Figs. 5.53 and 5.54. These models can be augmented by including the output resistance \( r_o = \frac{V_{CE}}{I_C} \) between the collector and the emitter. Table 5.4 provides a summary of the equations for determining the model parameters.

- Bias design seeks to establish a dc collector current that is as independent of the value of \( \beta \) as possible.

- In the common-emitter configuration, the emitter is at signal ground, the input signal is applied to the base, and the output is taken at the collector. A high voltage gain and a reasonably high input resistance are obtained, but the high-frequency response is limited.

- The input resistance of the common-emitter amplifier can be increased by including an unbypassed resistance in the emitter lead. This emitter-degeneration resistance provides other performance improvements at the expense of reduced voltage gain.

- In the common-base configuration, the base is at signal ground, the input signal is applied to the emitter, and the output is taken at the collector. A high voltage gain (from emitter to collector) and an excellent high-frequency response are obtained, but the input resistance is very low. The CB amplifier is useful as a current buffer.

- In the emitter follower the collector is at signal ground, the input signal is applied to the emitter, and the output is taken at the collector. A high voltage gain (from emitter to collector) and an excellent high-frequency response are obtained, but the input resistance is very low. The circuit is useful as a voltage buffer.

- The basic BJT logic inverter utilizes the cutoff and saturation modes of transistor operation. A saturated transistor has a large amount of minority-carrier charge stored in its base region and is thus slow to turn off.

- Table 5.5 shows the parameters utilized to characterize amplifiers.

- A summary of the characteristics of discrete single-stage BJT amplifiers, refer to Table 5.6.

- The high-frequency model of the BJT together with the formulas for determining its parameter values are shown in Table 5.7.
The doping concentrations are as follows: in the emitter $19 \times 10^{15}/\text{cm}^3$, in the base $10^{17}/\text{cm}^3$, and in the collector $10^{19}/\text{cm}^3$. The transistor is operating at $T = 300 \text{ K}$. For electronsdiffusing in the base, $D_n = 1.5 \times 10^{6}/\text{cm}^2/\text{s}$. For holesdiffusing in the emitter, $L_p = 19 \mu \text{m}$ and $D_p = 2.13 \times 10^5/\text{cm}^2/\text{s}$. For electronsentering the base, $L_e = 0.6 \mu \text{m}$ and $D_e = 1.7 \times 10^3/\text{cm}^2/\text{s}$. Calculate $L_e$ and $B$ assuming that the base-width $W$ is:

(a) $1 \mu \text{m}$  
(b) $2 \mu \text{m}$  
(c) $5 \mu \text{m}$

For case (b), if $I_e = 1 \text{ mA}$, find $I_n$, $I_p$, $V_{BE}$, and the minority-carrier charge stored in the base.

5.3 Two transistors, fabricated with the same technology but having different junction areas, when operated at a base-emitter voltage of $0.72 \text{ V}$, have collector currents of $0.2 \text{ mA}$ and $12 \text{ mA}$. Find $I_e$ for each device. What are the relative junction areas?

5.4 In a particular BJT, the base current is $7.5 \mu \text{A}$, and the collector current is $400 \mu \text{A}$. Find $B$ and $v$ for this device.

### PROBLEMS

**SECTION 5.1: DEVICE STRUCTURE AND PHYSICAL OPERATION**

5.1 The terminal voltages of various npn transistors are measured during operation in their respective circuits with the following results:

<table>
<thead>
<tr>
<th>Case</th>
<th>E (mV)</th>
<th>B (mA)</th>
<th>C (mA)</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0.7</td>
<td>0.7</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0.8</td>
<td>0.1</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>-0.7</td>
<td>0</td>
<td>0.7</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>-0.7</td>
<td>0</td>
<td>-0.6</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>0.7</td>
<td>0.7</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>-2.7</td>
<td>-2.0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>0</td>
<td>0</td>
<td>5.0</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>-0.10</td>
<td>5.0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

In this table, where the entries are in volts, 0 indicates the reference terminal to which the black (negative) probe of the voltmeter is connected. For each case, identify the mode of operation of the transistor.

5.2 An npn transistor has an emitter area of $10 \mu \text{m} \times 10 \mu \text{m}$. The doping concentrations are as follows: in the emitter $N_e = 10^{16}/\text{cm}^2$, in the base $N_b = 10^{15}/\text{cm}^2$, and in the collector $N_c = 10^{15}/\text{cm}^2$. The transistor is operating at $T = 300 \text{ K}$, where $n_e = 1.5 \times 10^{10}/\text{cm}^3$. For electrons diffusing in the base, $L_e = 19 \mu \text{m}$ and $D_e = 2.13 \times 10^5/\text{cm}^2/\text{s}$. For holes diffusing in the emitter, $L_p = 0.6 \mu \text{m}$ and $D_p = 1.7 \times 10^3/\text{cm}^2/\text{s}$. Calculate $L_e$ and $B$ assuming that the base-width $W$ is:

(a) $1 \mu \text{m}$  
(b) $2 \mu \text{m}$  
(c) $5 \mu \text{m}$

For case (b), if $I_e = 1 \text{ mA}$, find $I_n$, $I_p$, $V_{BE}$, and the minority-carrier charge stored in the base. (Hint: $\tau_e = L_e^2/D_e$. Recall that the electron charge $q = 1.6 \times 10^{-19}/\text{Coulomb}$.)

5.3 Two transistors, fabricated with the same technology but having different junction areas, when operated at a base-emitter voltage of $0.72 \text{ V}$, have collector currents of $0.2 \text{ mA}$ and $12 \text{ mA}$. Find $I_e$ for each device. What are the relative junction areas?

5.4 In a particular BJT, the base current is $7.5 \mu \text{A}$, and the collector current is $400 \mu \text{A}$. Find $B$ and $v$ for this device.

5.5 Find the values of $B$ that correspond to $v$ values of 0.5, 0.8, 0.9, 0.95, 0.99, and 0.999.

5.6 Find the values of $v$ that correspond to $B$ values of 1, 2, 10, 20, 100, 200, 1000, and 2000.

5.7 Measurement of $V_{BE}$ and two terminal currents taken on a number of npn transistors are tabulated below. For each, calculate the missing current value as well as $B$ and $v$ as indicated by the table.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>$V_{BE}$ (mV)</th>
<th>$I_e$ (mA)</th>
<th>$I_C$ (mA)</th>
<th>$I_B$ (mA)</th>
<th>$v$</th>
<th>$B$</th>
</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td>680</td>
<td>1.000</td>
<td>1.000</td>
<td>50</td>
<td>0.70</td>
<td>50</td>
</tr>
<tr>
<td>b</td>
<td>680</td>
<td>1.000</td>
<td>580</td>
<td>120</td>
<td>1.00</td>
<td>10</td>
</tr>
<tr>
<td>c</td>
<td>780</td>
<td>1.050</td>
<td>10</td>
<td>120</td>
<td>1.17</td>
<td>10</td>
</tr>
<tr>
<td>d</td>
<td>780</td>
<td>1.070</td>
<td>820</td>
<td>75.00</td>
<td>1.00</td>
<td>10</td>
</tr>
<tr>
<td>e</td>
<td>820</td>
<td>1.070</td>
<td>100</td>
<td>75.00</td>
<td>0.99</td>
<td>10</td>
</tr>
</tbody>
</table>

5.8 Consider an npn transistor whose base-emitter drop is $0.76 \text{ V}$ at a collector current of $10 \text{ mA}$. What current will it conduct at $v_{BE} = 0.70 \text{ V}$? What is its base-emitter voltage for $i_C = 10 \mu \text{A}$?

5.9 Show that for a transistor with $v$ close to unity, if $v$ changes by a small per-unit amount $\Delta v$, the corresponding per-unit change in $B$ is given approximately by $\frac{\Delta B}{B} = \frac{\Delta v}{v}$.

5.10 An npn transistor of a type whose $B$ is specified to range from 60 to 300 is connected in a circuit with emitter grounded, collector at $+9 \text{ V}$, and a current of $50 \mu \text{A}$ injected into the base. Calculate the range of collector and emitter currents that can result. What is the maximum power dissipated in the transistor? (Note: Perhaps you can see why this is a bad way to establish the collector operating current in a BJT.)

5.11 A particular BJT when conducting a collector current of $10 \mu \text{A}$ is known to have $v_{BE} = 0.70 \text{ V}$ and $I_B = 100 \mu \text{A}$. Use these data to create specific transistor models of the form shown in Figs. 5.5(a) and (b).
5.12 Using the npn transistor model of Fig. 5.5(b), consider
the case of a transistor for which the base is connected to
ground, the collector is connected to a 10-V dc source through
a 2-kΩ resistor, and a 3-mA current source is connected to the
emitter with the polarity so that current is drawn out of the
emitter terminal. If $\beta = 100$ and $I_S = 10^{-15}$ A, find the voltages
at the emitter and the collector and calculate the base current.

5.13 Consider an npn transistor for which $\beta_F = 100$,
$\alpha_R = 0.1$, and $I_S = 10^{-15}$ A.

(a) If the transistor is operated in the forward active mode
with $I_B = 10 \mu$A and $V_{CB} = 1$ V, find $V_{BE}$, $I_C$, and $I_E$.

(b) Now, operate the transistor in the reverse active mode
with a forward-bias voltage $V_{BC}$ equal to the value of $V_{BE}$
found in (a) and with $V_{EB} = 1$ V. Find $I_C$, $I_B$, and $I_E$.

5.14 A transistor characterized by the Ebers-Moll model
shown in Fig. 5.8 is operated with both emitter and collector
grounded and a base current of 1 mA. If the collector junction
is 10 times larger than the emitter junction and find $I_C$ and $I_E$.

*5.15 (a) Use the Ebers-Moll expressions in Eqs. (5.26)
and (5.27) to show that the $i_C$–$v_{CB}$ relationship sketched in
Fig. 5.9 can be described by

$$i_C = \alpha_R I_C - I_S \left( \frac{1}{\alpha_R} - \alpha_F \right) e^{-v_{BE}/VT}$$

(b) Calculate and sketch $i_C$–$v_{CB}$ curves for a transistor for
which $I_S = 10^{-15}$ A, $\alpha_R \approx 1$, and $\alpha_F = 0.1$. Sketch graphs for
each, give the values of $v_{BC}$, $v_{BE}$, and $v_{CE}$ for which
$i_C = 0.5 \alpha_F I_E$ and $i_C = 0$.

5.16 Consider the pnp large-signal model of Fig. 5.12(b)
applied to a transistor having $I_S = 10^{-17}$ A and $\beta = 40$. If the
emitter is connected to ground, the base is connected to a cur-
rent source that pulls out of the base terminal a current of
20 $\mu$A, and the collector is connected to a negative supply of
$-10$ V via a 10-kΩ resistor, find the collector voltage, the
emitter current, and the base voltage.

5.17 A pnp transistor has $V_{BE} = 0.8$ V at a collector current of
1 A. What do you expect $V_{BE}$ to become at $i_C = 10$ mA? At
$i_C = 5$ A?

5.18 A pnp transistor modeled with the circuit in Fig. 5.12 is
connected with its base at ground, collector at $-1.5$ V, and a
10-mA current injected into its emitter. If it is said to have
$\beta = 10$, what are its base and collector currents? In which
direction do they flow? If $I_C = 10^{-16}$ A, what voltage results at
the emitter? What does the collector current become if a tran-
sistor with $\beta = 1000$ is substituted? (Note: The fact that the
collector current changes by less than 10% for a large change of
$\beta$ illustrates that this is a good way to establish a specific
collector current.)

5.19 A pnp power transistor operates with an emitter-to-
collector voltage of 5 V, an emitter current of 10 A, and
$V_{EB} = 0.85$ V. For $\beta = 15$, what base current is required? What is
$I_C$ for this transistor? Compare the emitter–base junction
area of this transistor with that of a small-signal transistor
that conducts $I_C = 1$ mA with $V_{BE} = 0.70$ V. How much
larger is it?

SECTION 5.2: CURRENT-VOLTAGE
CHARACTERISTICS

5.20 For the circuits in Fig. P5.20, assume that the transis-
tors have very large $\beta$. Some measurements have been made
on these circuits, the results are indicated in the figure. Find
the values of the other labeled voltages and currents.

5.21 Measurements on the circuits of Fig. P5.21 produce
labeled voltages as indicated. Find the value of $\beta$ for each
transistor.

D5.22 Examination of the table of standard values for
resistors with 5% tolerance in Appendix X reveals that the
closest values to those found in the design of Example 5.1 are
$5.1 \, \text{kΩ}$ and $6.8 \, \text{kΩ}$. For these values use approximate calcula-
tions (e.g., $V_{BE} = 0.7 \, \text{V}$ and $\alpha = 1$) to determine the values
of collector current and collector voltage that are likely to
result.

D5.23 Redesign the circuit in Example 5.1 to provide
$V_C = +3 \, \text{V}$ and $I_C = 5 \, \text{mA}$.

5.24 For each of the circuits shown in Fig. P5.24, find the
emitter, base, and collector voltages and currents. Use
$\beta = 30$, but assume $V_{BE}$ and $V_C$ independent of current level.

5.25 Repeat Problem 5.24 using transistors for which
$V_{BE} = 0.7 \, \text{V}$ and $I_C = 1 \, \text{mA}$.

5.26 For the circuit shown in Fig. P5.26, measurement
indicates that $V_B = -1.5 \, \text{V}$. Assuming $V_{BE} = 0.7 \, \text{V}$, calculate
$V_E, \alpha, \beta$, and $V_C$. If a transistor with $\beta = \infty$ is used, what values
of $V_E, V_C$, and $V_B$ result?
5.27 The current $I_{E,0}$ of a small transistor is measured to be 20 nA at 25°C. If the temperature of the device is raised to 85°C, what do you expect $I_{E,0}$ to become?

5.28 Augment the model of the npn BJT shown in Fig. 5.20(a) by a current source representing $I_{E,0}$. In terms of this addition, what do the terminal currents $i_E$, $i_C$, and $i_B$ become? If the base lead is open-circuited while the emitter is connected to ground and the collector is connected to a positive supply, find the emitter and collector currents.

5.29 An npn transistor is accidentally connected with collector and emitter leads interchanged. The resulting currents in the normal emitter and base leads are 0.5 mA and 1 mA, respectively. What are the values of $q_n$ and $b_n^0$?

5.30 A BJT whose emitter current is fixed at 1 mA has a base-emitter voltage of 0.69 V at 25°C. What base-emitter voltage would you expect at 0°C? At 100°C?

5.31 A particular pnp transistor operating at an emitter current of 0.5 mA at 20°C has an emitter-base voltage of 602 mV. What does $V_{BE}$ become if the junction temperature rises to 50°C?

5.32 Consider a transistor for which the base-emitter voltage drop is 0.7 V at 10 mA. What current flows for $V_{BE} = 0.5$ V?

5.33 In Problem 5.32, the stated voltages are measured at 25°C. What values correspond at −25°C? At 125°C?

5.34 Use the Ebers-Moll expressions in Eqs. (5.31) and (5.32) to derive Eq. (5.35). Note that the emitter current is set to a constant value $I_E$. Ignore the terms not involving exponentials.

5.35 Use Eq. (5.35) to plot the $i_C = i_{CE}$ characteristics of an npn transistor having $q_n = 1$, $q_B = 0.1$, and $I_E = 10^{-15}$ A. Plot graphs for $I_E = 0.1$ mA, 0.5 mA, and 1 mA. Use an expanded scale for the negative values of $V_{CE}$ in order to show the details of the saturation region. Neglect the Early effect.

5.36 For the saturated transistor shown in Fig. P5.36, use the EM expressions to show that for $v_C = 1$,

$$V_{CE, sat} = V_T \ln \left( \frac{1}{a} \frac{I_C}{I_E} \right)$$

For a BJT with $a = 0.1$, evaluate $V_{CE, sat}$ for $I_C/I_E = 0.9$, 0.5, 0.1, and 0.

5.37 Use Eq. (5.36) to plot $i_C$ versus $V_{CE}$ for an npn transistor having $I_C = 10^{-15}$ A and $V_T = 100$ V. Provide curves for $V_{BE} = 0.60, 0.70, 0.72, 0.73,$ and 0.74 volts. Show the characteristics for $V_{BE}$ up to 15 V.

5.38 For a particular npn transistor operating at a $V_{BE}$ of 670 mV and $I_C = 3$ mA, the $i_C = i_{CE}$ characteristic has a slope of $3 \times 10^{-4}$. To what value of output resistance does this correspond? What is the value of the Early voltage for this transistor? For operation at 30 mA, what would the output resistance become?

5.39 For a BJT having an Early voltage of 200 V, what is its output resistance at 1 mA? At 100 μA?

5.40 Measurements of the $i_C = i_{CE}$ characteristic of a small-signal transistor operating at $V_{BE} = 720$ mV show that $i_C = 1.8$ mA at $V_{CE} = 2$ V and that $i_C = 2.4$ mA at $V_{CE} = 1.4$ V. What is the corresponding value of $i_C$ near saturation? At what value of $V_{CE}$ is $i_C = 2.0$ mA? What is the value of the Early voltage for this transistor? What is the output resistance that corresponds to operation at $V_{BE} = 720$ V?

5.41 Give the pnp equivalent circuit models that correspond to those shown in Fig. 5.20 for the npn case.

5.42 A BJT operating at $V_T = 8$ mA and $i_C = 1.2$ mA undergoes a reduction in base current of 0.8 μA. It is found that when $V_{BE}$ is held constant, the corresponding reduction in collector current is 0.1 mA. What are the values of $b_n$ and $h_{FE}$ that apply? If the base current is increased from 8 μA to 10 μA...
Since  IC
Find where value of temperature (four values needed).  

temperature coefficient for temperatures above and below room temperature (four values needed).

5.44 Figure P5.44 shows a diode-connected npn transistor. Since  VBE = 0 results in active-mode operation, the BJT will internally operate in the active mode; that is, its base and collector currents will be related by  β. Use the EM equations to show that the diode-connected transistor has the  i–v characteristics:

\[ i = \frac{I_C}{\alpha} \left( e^{V_T/I_0} - 1 \right) \equiv I_C e^{V_T/I_0} \]

\[ R_{CE} = \frac{V_{CE}}{i_C} \]

\[ R_{CE} \approx \frac{\alpha V_T}{\beta} \]

\[ s = \frac{V_T}{R_{CE}} = \frac{\alpha V_T}{\beta} \]

Find  R_{CE} for  β = \beta/2.

5.45 A BJT for which  α = 0.2 operates with a constant base current but with the collector open. What value of  V_{CEsat} would you measure?

5.46 Find the saturation voltage  V_{CEsat} and the saturation resistance  R_{CEsat} of an npn BJT operated at a constant base current of 0.1 mA and a forced  β of 20. The transistor has  β_0 = 50 and  β = 0.2. 

Note: Because here we are modeling operation at a very low forced  β, the value of  R_{CEsat} will be much larger than that given by Eq. 5.48).

5.47 A transistor has  β_0 = 150 and the collector junction is 10 times larger than the emitter junction. Evaluate  V_{CEsat} for  \beta_{sat}/\beta_0 = 0.99, 0.95, 0.9, 0.5, 0.1, 0.01, and 0.001.

5.50 A particular npn BJT with  V_{BE} = 720 mV at  I_C = 600 µA and, having  β = 150, has a collector-base junction 20 times larger than the emitter-base junction. 
(a) Find  α,  β_0, and  β. 
(b) For a collector current of 5 mA and nonsaturated operation, what is the base-emitter voltage and the base current?
(c) For the situation in (b) but with double the calculated base current, what is the value of forced  β? What are the base-emitter and base-collector voltages? 
5.51 A BJT with fixed base current has  V_{CEsat} = 60 mV with the emitter grounded and the collector open-circuited. When the collector is grounded and the emitter is open-circuited,  V_{CEsat} becomes –1 mV. Estimate values for  β_0 and  β for this transistor.

5.52 A BJT for which  I_C = 0.5 mA has  V_{CEsat} = 140 mV at  I_C = 10 mA and  V_{CEsat} = 170 mV at  I_C = 20 mA. Estimate the values of its saturation resistance,  R_{CEsat} and its offset voltage,  V_{CEoff}. Also, determine the values of  β_0 and  β for this transistor.

5.53 A BJT for which  V_{BE} = 30 V is connected as shown in Fig. P5.53. What voltages would you measure on the collector, base, and emitter?

FIGURE P5.44

SECTION 5.3: THE BJT AS AN AMPLIFIER AND AS A SWITCH

5.54 A common-emitter amplifier circuit operated with  V_{CC} = +10 V is biased at  V_{BE} = +1 V. Find the voltage gain, the maximum allowed output negative swing without the transistor entering saturation, and the corresponding maximum input signal permitted.

5.55 For the common-emitter circuit in Fig. 5.26(a) with  V_{CC} = +10 V and  R_E = 1 kΩ, find  V_{CE} and the voltage gain of the following dc collector bias currents: 1 mA, 2 mA, 5 mA, 8 mA, and 9 mA. For each, give the maximum possible positive and
negative-output-signal swing as determined by the need to keep
the transistor in the active region. Present your results in a table.

D5.56 Consider the CE amplifier circuit of Fig. 5.26(a)
when operated with a dc supply $V_{CC} = +5 \, \text{V}$. It is required to
find the point at which the transistor should be biased; that
is, find the value of $V_{CE}$ so that the output sine-wave signal $V_o$ resulting from an input sine-wave signal $V_i$ of 5-mV
peak amplitude has the maximum possible magnitude. What
is the peak amplitude of the output sine wave and the value
of the gain obtained? Assume linear operation around the
bias point. (Hint: To obtain the maximum possible output
amplitude for a given input, you need to bias the transistor
as close to the edge of saturation as possible without enter-
ing saturation at any time, that is, without $v_{CE}$ decreasing
below 0.3 \, \text{V}.)

5.57 The transistor in the circuit of Fig. P5.57 is biased at a
dc collector current of 0.5 mA. What is the voltage gain?
(Hint: Use the Thévenin theorem to convert the circuit to the
form in Fig. 5.26(a).)

\[ v_{CE} = I_{C} R_C \]

\[ v_{BE} = V_{BE} - I_{C} R_E \]

\[ \beta = \frac{I_C}{I_B} \]

For the case $V_{CE} = 5 \, \text{V}$ and $V_{CE} = 2.5 \, \text{V}$, what is the gain
without and with the Early effect taken into account? Let
$V_i = 100 \, \text{V}.$

5.60 When the common-emitter amplifier circuit of
Fig. 5.26(a) is biased with a certain $V_{BE}$, dc voltage at the
collector was found to be $+2 \, \text{V}$. For $V_{CC} = +5 \, \text{V}$ and $R_C = 1 \, \Omega$,
find $I_C$ and the small-signal voltage gain. For a
change $\Delta V_{BE} = +5 \, \text{mV}$, calculate the resulting $\Delta I_C$. Calculate
it two ways: by finding $\Delta I_C$ using the transistor exponential
characteristic and approximately using the small-signal
voltage gain. Repeat for $\Delta V_{BE} = -5 \, \text{mV}.$ Summarize your
results in a table.

*5.61 Consider the common-emitter amplifier circuit of
Fig. 5.26(a) when operated with a supply voltage $V_{CC} = +5 \, \text{V}.$

(a) What is the theoretical maximum voltage gain that this
amplifier can provide?

(b) What value of $V_{CE}$ must this amplifier be biased at to pro-
vide a voltage gain of $-100 \, \text{V/V}$?

(c) If the dc collector current $I_C$ at the bias point is to be
0.5 mA, what value of $R_C$ should be used?

(d) What is the value of $V_{CE}$ required to provide the bias point
mentioned above? Assume that the BJT has $I_C = 10^{-5} \, \text{A}.$

(e) If a sine-wave signal $v_{BE}$ having a 5-mV peak amplitude is
superimposed on $V_{BE}$, find the corresponding output voltage
signal $v_{CE}$ that will be superimposed on $V_{CE}$ assuming linear
operation around the bias point.

(f) Characterize the signal current $i_C$ that will be super-
imposed on the dc bias current $I_C$.

(g) What is the value of the dc base current $I_B$ at the bias
point. Assume $\beta = 100.$ Characterize the signal current $i_B$ that
will be superimposed on the base current $I_B$.

(h) Dividing the amplitude of $v_{BE}$ by the amplitude of $i_C$, evalu-
ate the incremental (or small-signal) input resistance of the
amplifier

(i) Sketch and clearly label correlated graphs for $v_{BE}$, $v_{CE}$, $I_C$, and
$I_B$. Note that each graph consists of a dc or average value
and a superimposed sine wave. Be careful of the phase rela-
tionships of the sine waves.
5.62 The essence of transistor operation is that a change in $v_{BC}$, $\Delta v_{BC}$, produces a change in $i_C$, $\Delta i_C$. By keeping $\Delta v_{BC}$ small, $\Delta i_C$ is approximately linearly related to $\Delta v_{BC}$, $\Delta i_C \approx g_m \Delta v_{BC}$, where $g_m$ is known as the transistor transconductance. By passing $\Delta i_C$ in $R_C$, an output voltage signal $\Delta v_C$ is obtained. Use the expression for the small-signal voltage gain in Eq. (5.56) to derive an expression for $g_m$. Find the value of $g_m$ for a transistor biased at $I_E = 1$ mA.

5.63 Consider the characteristic curves shown in Fig. 5.29 with the following additional calibration data: Label, from the lowest colored line, $i_E = 1 \mu A$, 10 $\mu A$, 20 $\mu A$, 30 $\mu A$, and 40 $\mu A$. Assume the lines to be horizontal, and let $\beta = 100$.

For $V_{CC} = 5$ V and $R_E = 1$ k$\Omega$, what peak-to-peak collector voltage swing will result for $I_E$ varying over the range 10 $\mu A$ to 40 $\mu A$? If at the bias point (not the one shown in the figure) $V_{CE} = \frac{1}{2}V_{CC}$, find the value of $I_C$ and $I_E$. If at this current $V_{CC} = 0.7$ V and if $R_E = 100$ k$\Omega$, find the required value of $V_{BE}$.

*5.64 Sketch the $i_C$-$v_{BC}$ characteristics of an npn transistor having $\beta = 100$ and $V_T = 100$ V. Sketch characteristic curves for $i_E = 20$ $\mu A$, 50 $\mu A$, 100 $\mu A$. For the purpose of this sketch, assume that $i_C = \beta i_E$ at $v_{BC} = 0$. Also, sketch the load line obtained for $V_{CC} = 10$ V and $R_E = 1$ k$\Omega$. If the dc bias current into the base is 50 $\mu A$, write the equation for the corresponding $i_E$-$v_{BC}$ curve. Also, write the equation for the load line, and solve the two equations to obtain $i_C$ and $I_E$. If the input signal causes a sinusoidal signal of 30-\mu A peak amplitude to be superimposed on $I_E$, find the corresponding signal components of $i_C$ and $v_{BC}$.

D5.65 For the circuit in Fig. P5.65 select a value for $R_E$ so that the transistor saturates with an overdrive factor of 10. The BJT is specified to have a minimum $\beta$ of 20 and $V_{CEsat} = 0.2$ V. What is the value of forced $\beta$ achieved?

D5.66 For the circuit in Fig. P5.66 select a value for $R_E$ so that the transistor saturates with a forced $\beta$ of 10. Assume $V_{BE} = 0.7$ V and $V_{CEsat} = 0.2$ V.

*5.67 For each of the saturated circuits in Fig. P5.67, find $i_E$, $i_C$, and $i_B$. Use $V_{BE} = 0.7$ V and $V_{CEsat} = 0.2$ V.

*5.68 Consider the operation of the circuit shown in Fig. P5.68 as $v_{BC}$ rises slowly from zero. For this transistor, assume $\beta = 50$. $v_{BC}$ at which the transistor conducts is 0.5 V, $v_{BE}$ when fully conducting is 0.7 V, saturation begins at $v_{BC} = 0.4$ V, and the transistor is deeply in saturation at $v_{BC} = 0.6$ V. Sketch and label $v_{BC}$ and $i_C$ versus $i_E$. For what range of $v_{BC}$ is $i_C$ essentially zero? What are the values of $v_{BC}$, $i_E$, $i_C$, and $v_{BE}$? Augment your sketch by adding a plot of $i_B$.
CHAPTER 5  BIPOLAR JUNCTION TRANSISTORS (BJTs)

SECTION 5.4: BJT CIRCUITS AT DC

5.69 The transistor in the circuit of Fig. P5.69 has a very high β. Find \( V_E \) and \( V_C \) for \( V_B \) (a) +2 V, (b) +1 V, and (c) 0 V. Assume \( V_{BE} \approx 0.7 \) V.

5.70 The transistor in the circuit of Fig. P5.69 has a very high β. Find the highest value of \( V_B \) for which the transistor still operates in the active mode. Also, find the value of \( V_B \) for which the transistor operates in saturation with a forced β of 1.

5.71 Consider the operation of the circuit shown in Fig. P5.71 for \( V_B \) at –1 V, 0 V, and +1 V. Assume that \( V_{BE} \approx 0.7 \) V for usual currents and that β is very high. What values of \( V_C \) and \( V_E \) result? At what value of \( V_B \) does the emitter current reduce to one-tenth of its value for \( V_B = 0 \) V? For what value of \( V_B \) is the transistor just at the edge of conduction? What values of \( V_E \) and \( V_C \) correspond? For what value of \( V_B \) does the transistor reach saturation (when the base-to-collector junction reaches 0.5 V of forward bias)? What values of \( V_C \) and \( V_E \) correspond? Find the value of \( V_E \) for which the transistor operates in saturation with a forced β of 2.

5.72 For the transistor shown in Fig. P5.72, assume \( \alpha \approx 1 \) and \( V_{BE} = 0.5 \) V at the edge of conduction. What are the values of \( V_E \) and \( V_C \) for \( V_B = 0 \) V? For what value of \( V_B \) does the transistor cut off? Saturate? In each case, what values of \( V_E \) and \( V_C \) result?

5.73 Consider the circuit in Fig. P5.69 with the base voltage \( V_B \) obtained using a voltage divider across the 5-V supply. Assuming the transistor β to be very large (i.e., ignoring the base current), design the voltage divider to obtain \( V_B = 2 \) V. Design for a 0.2-mA current in the voltage divider. Now, if the BJT \( \beta = 100 \), analyze the circuit to determine the collector current and the collector voltage.
5.74 A single measurement indicates the emitter voltage of the transistor in the circuit of Fig. P5.74 to be 1.0 V. Under the assumption that $V_{BE} = 0.7$ V, what are $V_B$, $I_B$, $I_E$, $I_C$, $V_C$, $\beta$ and $\alpha$? (Note: Isn’t it surprising what a little measurement can lead to?)

5.77 In the circuit shown in Fig. P5.76, the transistor has $\beta = 30$. Find the values of $V_B$, $V_C$, and $V_E$ and verify that the transistor is operating in the active mode. What is the largest value that $R_E$ can have while the transistor remains in the active mode?

5.78 For the circuit in Fig. P5.78, find $V_B$, $V_C$, and $V_E$ for $R_E = 100$ kΩ, 10 kΩ, and 1 kΩ. Let $\beta = 100$.

5.79 For the circuits in Fig. P5.79, find values for the labeled node voltages and branch currents. Assume $\beta$ to be very high and $V_{BE} = 0.7$ V.

5.80 Repeat the analysis of the circuits in Problem 5.79 using $\beta = 100$. Find all the labeled node voltages and branch currents. Assume $V_{BE} = 0.7$ V.

**D5.81** It is required to design the circuit in Fig. P5.81 so that a current of 1 mA is established in the emitter and a voltage of +5 V appears at the collector. The transistor type used has a nominal $\beta$ of 100. However, the $\beta$ value can be as low as 50 and as high as 150. Your design should ensure that the specified emitter current is obtained when $\beta = 100$ and that at the extreme values of $\beta$ the emitter current does not change by more than 10% of its nominal value. Also, design for as large a value for $R_E$ as possible. Give the values of $R_E$, $R_C$, and $R_B$ to the nearest kilohm. What is the expected range of collector current and collector voltage corresponding to the full range of $\beta$ values?

5.82 The pnp transistor in the circuit of Fig. P5.82 has $\beta = 50$. Find the value for $R_E$ to obtain $V_E = +5$ V. What happens if the transistor is replaced with another having $\beta = 100$?
CHAPTER 5  BIPOLAR JUNCTION TRANSISTORS (BJTs)

![Diagram of Bipolar Junction Transistors (BJTs)](image)

**FIGURE P5.79**

**FIGURE P5.81**

**FIGURE P5.82**
**5.83** Consider the circuit shown in Fig. P5.83. It resembles that in Fig. 5.41 but includes other features. First, note diodes $D_1$ and $D_2$ are included to make design (and analysis) easier and to provide temperature compensation for the emitter-base voltages of $Q_1$ and $Q_2$. Second, note resistor $R$, whose purpose is to provide negative feedback (more on this later in the book). Using $I_{D}=0$ and $V_{D}=0.7 \, \text{V}$ independent of current and $\beta=\infty$, find the voltages $V_{B_1}, V_{E_1}, V_{C_1}, V_{B_2}, V_{E_2},$ and $V_{C_2}$, initially with $R$ open-circuited and then with $R$ connected. Repeat for $\beta=100$, initially with $R$ open-circuited then connected.

**5.84** For the circuit shown in Fig. P5.84, find the labeled node voltages for:
(a) $\beta=\infty$
(b) $\beta=100$

**5.85** Using $\beta=\infty$, design the circuit shown in Fig. P5.85 so that the bias currents in $Q_1$, $Q_2$, and $Q_3$ are 2 mA, 2 mA, and 4 mA, respectively, and $V_1=0$, $V_2=-4 \, \text{V}$, and $V_3=2 \, \text{V}$. For each resistor, select the nearest standard value utilizing the table of standard values for 5% resistors in Appendix H. Now, for $\beta=100$, find the values of $V_3$, $V_4$, $V_5$, $V_6$, and $V_7$.

**5.86** For the circuit in Fig. P5.86, find $V_8$ and $V_9$ for $V_i=0 \, \text{V}$, $+3 \, \text{V}$, $-5 \, \text{V}$, and $-10 \, \text{V}$. The BJTs have $\beta=100$.

**5.87** Find the approximate values for the collector voltages in the circuits of Fig. P5.87. Also, calculate forced $\beta$ for each of the transistors. (Hint: Assume all transistors are operating in saturation, and verify the assumption.)
FIGURE P5.87

SECTION 5.5: BIASING IN BJT AMPLIFIER CIRCUITS

D5.88 For the circuit in Fig. 5.43(a), neglect the base current $I_B$ in comparison with the current in the voltage divider. It is required to bias the transistor at $I_C = 1\, mA$, which requires selecting $R_E$ and $R_C$ so that $V_{BE} = 0.690\, V$. If $V_{CC} = 5\, V$, what must the ratio $R_C/R_E$ be? Now, if $R_E$ and $R_C$ are 1% resistors, that is, each can be in the range of 0.99 to 1.01 of its nominal value, what is the range obtained for $V_{BE}$? What is the corresponding range of $I_C$? If $R_C = 3\, k\Omega$, what is the range obtained for $V_{BE}$? Comment on the efficacy of this biasing arrangement.

D5.89 It is required to bias the transistor in the circuit of Fig. 5.43(b) at $I_C = 1\, mA$. The transistor $\beta$ is specified to be nominally 100, but it can fall in the range of 50 to 150. For $V_{CC} = +5\, V$ and $R_E = 3\, \Omega$, find the required ratio of $R_E$ to $R_C$ to achieve $I_C = 1\, mA$ for the “nominal” transistor. What is the expected range for $I_C$ and $V_{BE}$? Comment on the efficacy of this bias design.

D5.90 Consider the single-supply bias network shown in Fig. 5.44(a). Provide a design using a 9-V supply in which the supply voltage is equally split between $R_E$, $V_{CC}$, and $R_C$. With a collector current of 3 mA. The transistor $\beta$ is specified to have a minimum value of 90. Use a voltage-divider current which is $I_C/2$. Check your design at $\beta = 90$. If you have the data available, find how low $\beta$ can be while the value of $I_C$ does not fall below that obtained with the design of Problem 5.90 for $\beta = 90$.

**D5.91** It is required to design the bias circuit of Fig. 5.44 for a BJT whose nominal $\beta = 100$.

(a) Find the largest ratio $(R_E/R_C)$ that will guarantee $I_C$ remain within ±5% of its nominal value for $\beta$ as low as 50 and as high as 150.

(b) If the resistance ratio found in (a) is used, find an expression for the voltage $V_{BE} = V_{CC}/(R_E + R_C)$ that will result in a voltage drop of $V_{BE}/3$ across $R_C$. For $V_{CC} = 10\, V$, find the required values of $R_E$, $R_C$, and $R_B$ to obtain $I_C = 2\, mA$ and to satisfy the requirement for stability of $I_C$ in (a).

(c) For $V_{CC} = 3\, V$ and for $\beta = 90$, find the required values of $R_E$, $R_C$, and $R_B$.

(d) Find $R_B$ so that $V_{BE} = 3\, V$ for $\beta$ equal to its nominal value. Check your design by evaluating the resulting range of $I_C$.

*DS5.93* Consider the two-supply bias arrangement shown in Fig. 5.45 using ±3-V supplies. It is required to design the circuit so that $I_C = 3\, mA$ and $V_C$ is placed midway between $V_C^+$ and $V_C^-$. For $\beta = \infty$, what values of $R_A$ and $R_B$ are required?

(b) If the BJT is specified to have a minimum $\beta$ of 90, find the largest value for $R_A$ consistent with the need to limit the voltage drop across it to one-tenth the voltage drop across $R_C$.

(c) What standard 5%-resistor values (see Appendix X) would you use for $R_E$, $R_C$, and $R_A$? In making the selection, use somewhat lower values in order to compensate for the low-$\beta$ effects.

(d) For the values you selected in (c), find $I_C$, $V_A$, $V_B$, and $V_C$ for $\beta = \infty$ and for $\beta = 90$. 
**D5.94** Utilizing ±5-V power supplies, it is required to design a version of the circuit in Fig. 5.45 in which the signal will be coupled to the emitter and thus $R_E$ can be set to zero. Find values for $R_E$ and $R_C$ so that a dc emitter current of 1 mA is obtained and so that the gain is maximized while allowing ±1 V of signal swing at the collector. If temperature increases from the nominal value of 25°C to 125°C, estimate the percentage change in collector bias current. In addition to the ~2 mV/°C change in $V_{BE}$, assume that the transistor $\beta$ changes over this temperature range from 50 to 150.

**D5.95** Using a 5-V power supply, design a version of the circuit of Fig. 5.46 to provide a dc emitter current of 0.5 mA and to allow a ±1-V signal swing at the collector. The BJT has a nominal $\beta = 100$. Use standard 5%-resistor values (see Appendix H). If the actual BJT used has $\beta = 50$, what emitter current is obtained? Also, what is the allowable signal swing at the collector? Repeat for $\beta = 150$.

**D5.96** (a) Using a 3-V power supply, design the feedback bias circuit of Fig. 5.46 to provide $I_C = 3$ mA and $\beta = 90$.
(b) Select standard 5% resistor values, and reevaluate $V_C$ and $I_C$ for $\beta = 90$.
(c) Find $V_C$ and $I_C$ for $\beta = \infty$.
(d) To improve the situation that obtains when high-$\beta$ transistors are used, we have to arrange for an additional current to flow through $R_B$. This can be achieved by connecting a resistor between base and emitter, as shown in Fig. P5.96. Design this circuit for $\beta = 90$. Use a current through $R_B$ equal to the base current. Now, what values of $V_C$ and $I_C$ result with $\beta = \infty$?

**D5.97** A circuit that can provide a very large voltage gain for a high-resistance load is shown in Fig. P5.97. Find the values of $I$ and $R_B$ to bias the BJT at $I_E = 3$ mA and $V_C = 1.5$ V. Let $\beta = 90$.

**D5.98** The circuit in Fig. P5.98 provides a constant current $I_O$ as long as the circuit to which the collector is connected maintains the BJT in the active mode. Show that

$$I_O = \frac{V_{CC}(R_2/(R_1+R_2)) - V_{BE}}{R_1 + (R_1/R_2)/(\beta + 1)}$$

**D5.99** The current-bias circuit shown in Fig. P5.99 provides bias current to $Q_1$ that is independent of $R_4$ and nearly independent of the value of $\beta_1$ (as long as $Q_1$ operates in the active mode). Prepare a design meeting the following specifications: Use ±5-V supplies; $I_{E1} = 0.1$ mA, $V_{CC1} = 2$ V for $\beta = \infty$; the voltage across $R_2$ decreases by at most 5% for $\beta = 50$; $V_{CC1} = 1.5$ V for $\beta = \infty$ and 2.5 V for $\beta = 50$. Use standard 5%-resistor values (see Appendix H). What values for $R_1, R_2, R_4$, and $R_6$ do you choose? What values of $I_{E1}$ and $V_{CC1}$ result for $\beta = 90, 100,$ and 200?
For the circuit in Fig. P5.100, assuming all transistors to be identical with $\beta$ infinite, derive an expression for the output current $I_O$, and show that by selecting $R_2$ and keeping the current in each junction the same, the current $I_O$ will be which is independent of $V_{BE}$. What must the relationship of $R_E$ to $R_1$ and $R_2$ be? For $V_{CC} = 10 \text{ V}$ and assuming $\alpha = 1$ and $V_{BE} = 0.7 \text{ V}$, design the circuit to obtain an output current of 0.5 $\text{mA}$. What is the lowest voltage that can be applied to the collector of $Q_3$?

For the circuit in Fig. P5.101 find the value of $R$ that will result in $I_O = 2 \text{ mA}$. What is the largest voltage that can be applied to the collector? Assume $V_{BE} = 0.7 \text{ V}$.

Section 5.6: Small-Signal Operation and Models

Consider a transistor biased to operate in the active mode at a dc collector current $I_C$. Calculate the collector signal current as a fraction of $I_C$ (i.e., $I_c/I_C$) for input signals $v_{be}$ of $+1 \text{ mV}$, $-1 \text{ mV}$, $+2 \text{ mV}$, $-2 \text{ mV}$, $+5 \text{ mV}$, $-5 \text{ mV}$, $+8 \text{ mV}$, $-8 \text{ mV}$, $+10 \text{ mV}$, $-10 \text{ mV}$, $+12 \text{ mV}$, and $-12 \text{ mV}$. In each case do the calculation two ways:

(a) using the exponential characteristic, and
(b) using the small-signal approximation.

Present your results in the form of a table that includes a column for the error introduced by the small-signal approximation. Comment on the range of validity of the small-signal approximation.

An npn BJT with grounded emitter is operated with $V_{BE} = 0.700 \text{ V}$, at which the collector current is 1 $\text{mA}$. A 10-k$\Omega$ resistor connects the collector to a $+15 \text{ V}$ supply. What is the resulting collector voltage $V_C$? Now, if a signal applied to the base raises $v_{be}$ to 705 mV, find the resulting total collector current $i_C$ and total collector voltage $V_C$ using the exponential ($I_c=I_{oc}$) relationship. For this situation, what are $\alpha_r$, and $\epsilon_r$? Calculate the voltage gain $v_C/v_{be}$. Compare with the value obtained using the small-signal approximation, that is, $-\epsilon_r R_C$. A transistor with $\beta = 120$ is biased to operate at a dc collector current of 1.2 $\text{mA}$. Find the values of $g_{m}$, $r_e$, and $r_v$. Repeat for a bias current of 120 $\mu\text{A}$.

A pnp BJT biased to operate at $I_C = 2.0 \text{ mA}$. What is the associated value of $g_{m}$? If $\beta = 50$, what is the value of $r_v$?
the small-signal resistance seen looking into the emitter \((r_e)\)?

Into the base \((r_\pi)\)? If the collector is connected to a 5-k\(\Omega\) load, with a signal of 5-mV peak applied between base and emitter, what output signal voltage results?

\[5.106\]
A designer wishes to create a BJT amplifier with a \(g_m\) of 50 mA/V and a base input resistance of 2000 \(\Omega\) or more. What emitter-bias current should he choose? What is the minimum \(\beta\) he can tolerate for the transistor used?

\[5.107\]
A transistor operating with nominal \(g_m\) of 60 mA/V has a \(\beta\) that ranges from 50 to 200. Also, the bias circuit, being less than ideal, allows a \(\pm 20\%\) variation in \(I_C\). What are the extreme values found of the resistance looking into the base?

\[5.108\]
In the circuit of Fig. 5.48, \(V_{BE}\) is adjusted so that \(V_C = 2\) V. If \(V_{CC} = 5\) V, \(R_C = 3\) k\(\Omega\), and a signal \(V_{be} = 0.005\) sin \(\omega t\) volts is applied, find expressions for the total instantaneous quantities \(i_C(t), v_C(t),\) and \(i_B(t)\). The transistor has \(\beta = 100\). What is the voltage gain?

\[5.109\]
We wish to design the amplifier circuit of Fig. 5.48 under the constraint that \(V_{CC}\) is fixed. Let the input signal \(V_{be} = V_{m}\) sin \(\omega t\), where \(V_{m}\) is the maximum value for acceptable linearity. Show for the design that results in the largest signal at the collector without the BJT leaving the active region, that

\[
R_C I_C = \left(V_C - V_{BE} - 0.3 - V_T + \frac{V_{m}}{V_T}ight) \left(1 + \frac{V_{m}}{V_T}ight)
\]

and find an expression for the voltage gain obtained. For \(V_{CC} = 5\) V and \(V_{be} = 5\) mV, find the dc voltage at the collector, the amplitude of the output voltage signal, and the voltage gain.

\[5.110\]
The following table summarizes some of the basic attributes of a number of BJTs of different types, operating as amplifier under various conditions. Provide the missing entries.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>a</th>
<th>b</th>
<th>c</th>
<th>d</th>
<th>e</th>
<th>f</th>
<th>g</th>
</tr>
</thead>
<tbody>
<tr>
<td>(\alpha)</td>
<td>1.00</td>
<td>0.90</td>
<td>−</td>
<td>1.00</td>
<td>5</td>
<td>1.10</td>
<td>700</td>
</tr>
<tr>
<td>(\beta)</td>
<td>100</td>
<td>1.00</td>
<td>1.00</td>
<td>0.020</td>
<td>25</td>
<td>10.1 k(\Omega)</td>
<td></td>
</tr>
<tr>
<td>(I_C) (mA)</td>
<td>1.00</td>
<td>0.00</td>
<td>1.00</td>
<td>1.10</td>
<td>100</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>(I_B) (mA)</td>
<td>0.5 mA</td>
<td>0.5 mA</td>
<td>0.5 mA</td>
<td>0.5 mA</td>
<td>0.5 mA</td>
<td>0.5 mA</td>
<td></td>
</tr>
<tr>
<td>(g_{m}) (mA/V)</td>
<td>50 mA/V</td>
<td>50 mA/V</td>
<td>50 mA/V</td>
<td>50 mA/V</td>
<td>50 mA/V</td>
<td>50 mA/V</td>
<td></td>
</tr>
<tr>
<td>(r_e) ((\Omega))</td>
<td>50 (\Omega)</td>
<td>100 (\Omega)</td>
<td>100 (\Omega)</td>
<td>100 (\Omega)</td>
<td>100 (\Omega)</td>
<td>100 (\Omega)</td>
<td></td>
</tr>
</tbody>
</table>

(Note: Isn’t it remarkable how much two parameters can reveal?)
2.5 kΩ. Draw the complete amplifier model using the hybrid-π BJT equivalent circuit. Calculate the overall voltage gain \((v_o/v_i)\). What is the value of BJT \(\beta\) implied by the values of the model parameters? To what value must \(\beta\) be increased to double the overall voltage gain?

5.115 For the circuit shown in Fig. P5.115, draw a complete small-signal equivalent circuit utilizing an appropriate \(T\) model for the BJT \((\alpha = 0.99)\). Your circuit should show the values of all components, including the model parameters. What is the input resistance \(R_{i}\)? Calculate the overall voltage gain \((v_o/v_i)\).

5.116 In the circuit shown in Fig. P5.116, the transistor has a \(\beta\) of 200. What is the dc voltage at the collector? Find the input resistances \(R_{in}\) and \(R_{o}\) and the overall voltage gain \((v_o/v_i)\). For output signal of 10.4 V, what values of \(v_i\) and \(v_o\) are required?

5.117 Consider the augmented hybrid-π model shown in Fig. 5.58. Disregarding how biasing is to be done, what is the largest possible voltage gain available for a signal source connected directly to the base and a very-high-resistance load? Calculate the value of the maximum possible gain for \(V_C = 25\) V and \(V_V = 250\) V.

5.118 Reconsider the amplifier shown in Fig. 5.53 and analyzed in Example 5.14 under the condition that \(\beta\) is not well controlled. For what value of \(\beta\) does the circuit begin to saturate? We can conclude that large \(\beta\) is dangerous in this circuit. Now, consider the effect of reduced \(\beta\), say, to \(\beta = 25\). What values of \(r_e, r_o,\) and \(v_o\) result? What is the overall voltage gain? (Note: You can see that this circuit, using base-current control of bias, is very \(\beta\)-sensitive and usually not recommended.)

5.119 Reconsider the circuit shown in Fig. 5.55 under the condition that the signal source has an internal resistance of 100 \(\Omega\). What does the overall voltage gain become? What is the largest input signal voltage that can be used without output-signal clipping?

5.120 Redesign the circuit of Fig. 5.55 by raising the resistor values by a factor \(n\) to increase the resistance seen by the input \(v_i\) to 75 \(\Omega\). What value of voltage gain results? Grounded-base circuits of this kind are used in systems such as cable TV, in which, for highest-quality signaling, load resistances need to be “matched” to the equivalent resistances of the interconnecting cables.

5.121 Using the BJT equivalent circuit model of Fig. 5.52(a), sketch the equivalent circuit of a transistor amplifier for which a resistance \(R_e\) is connected between the emitter and ground, the collector is grounded, and an input signal source \(v_s\) is connected between the base and ground. (It is assumed that the transistor is properly biased to operate in the active region.) Show that:

(a) the voltage gain between base and emitter, that is, \((v_e/v_b)\), is given by

\[
\frac{v_e}{v_b} = \frac{R_e}{R_1 + r_o}
\]

(b) the input resistance,

\[
R_{in} = \frac{R_1 + r_o}{n}
\]

Find the numerical values for \((v_e/v_b)\) and \(R_{in}\) for the case \(R_1 = 1\) k\(\Omega\), \(\beta = 100\), and the emitter bias current \(I_E = 1\) mA.

5.122 When the collector of a transistor is connected to its base, the transistor still operates (internally) in the active region because the collector-base junction is still in effect reverse biased. Use the simplified hybrid-π model to find the
incremental (small-signal) resistance of the resulting two-terminal device (known as a diode-connected transistor).

**5.123** Design an amplifier using the configuration of Fig. 5.55(a). The input signal source has a value of 10 V. The input signal source has a resistance of 100 kΩ, and it is required that the amplifier input resistance match this value. (Note that \( R_{\text{in}} = r_i \) if \( R_{\text{in}} = r_i \).) The amplifier is to have the greatest possible voltage gain and the largest possible output resistance. Find values for \( R_1 \) and \( R_2 \). What is the value of voltage gain realized?

**5.124** The transistor in the circuit shown in Fig. P5.124 is biased to operate in the active mode. Assuming that \( \beta \) is very large, find the collector bias current \( I_C \). Replace the transistor with the small-signal equivalent circuit model of Fig. 5.52(b) (remember to replace the dc power supply with a short circuit). Analyze the resulting amplifier equivalent circuit to show that

\[
\frac{v_o}{v_i} = \frac{R_C}{R_{\text{sig}}}.
\]

Find the values of these voltage gains \( (\alpha = 1) \). Now, if the terminal labeled \( v_{c_e} \) is connected to ground, what does the voltage gain \( \frac{v_o}{v_i} \) become?

**5.125** An amplifier is measured to have \( R_{\text{in}} = 10 \, \text{kΩ} \), \( A_{\text{in}} = 100 \, \text{V/V} \), and \( R_L = 100 \, \text{Ω} \). Also, when a load resistance \( R_L \) of 1 kΩ is connected between the output terminals, the input resistance is found to decrease to 8 kΩ. If the amplifier is fed with a signal source having an internal resistance of 2 kΩ, find \( G_m \), \( A_{\text{in}} \), \( G_{\text{dc}} \), \( A_{\text{out}} \), and \( A \).

**5.126** Figure P5.126 shows an alternative equivalent circuit for representing any linear two-port network including voltage amplifiers. This equivalent circuit is based on the \( g \)-parameter two-port representation (see Appendix X).

(a) Using the values of \( R_L \), \( A_{\text{in}} \), and \( R_{\text{out}} \) given in Example 5.17 together with the measured value of \( R_{\text{out}} \), 400 kΩ obtained when a load \( R_L \) of 10 kΩ is connected to the output, determine the value of the feedback factor \( f \).

(b) Now, use the equivalent circuit of Fig. P5.126 to determine the value of \( R_{\text{out}} \) obtained when the amplifier is fed with a signal generator having \( R_{\text{sig}} = 100 \, \text{kΩ} \). Check your result against that found in Example 5.17.

**5.127** Refer to Table 5.5. By equating the expression for \( G \), obtained from Equivalent Circuit A to that obtained from Equivalent Circuit B with \( G_{\text{in}} = R_{\text{in}}/(R_{\text{in}} + R_{\text{out}})A_{\text{in}} \), show that

\[
G = \frac{R_{\text{in}} + R_{\text{out}}}{R_{\text{in}}} \frac{R + R_{\text{out}}}{R_{\text{in}}} \frac{R}{R_{\text{out}} + R}
\]

Now, use this expression to:

(a) Show that for \( R_{\text{out}} \rightarrow \infty \), \( A_{\text{in}} \rightarrow R_{\text{in}} \).

(b) Show that for \( R_{\text{out}} = 0, R_{\text{in}} \rightarrow R_{\text{out}} \).

(c) Find \( R_{\text{out}} \) when \( R_{\text{in}} = \infty \) (i.e., the amplifier input is open-circuited), and evaluate its value for the amplifier specified in Example 5.17.

**5.128** A common-emitter amplifier of the type shown in Fig. 5.60(a) is biased to operate at \( I_C = 0.2 \, \text{mA} \) and has a collector resistance \( R_C = 24 \, \text{kΩ} \). The transistor has \( \beta = 100 \) and a large \( V_T \). The signal source is directly coupled to the base, and \( C_{\text{BJT}} \) and \( R_{\text{C}} \) are eliminated. Find \( R_{\text{in}} \), the voltage gain \( A_{\text{in}} \), and \( R_{\text{C}} \). Use these results to determine the overall voltage gain when a 10-kΩ load resistor is connected to the collector and the source resistance \( R_{\text{out}} = 10 \, \text{kΩ} \).

**5.129** Repeat Problem 5.128 with a 125-Ω load included in the signal path in the emitter. Furthermore, contrast the maximum amplitude of the input sine wave that can be applied with and without \( R_L \) assuming that to limit distortion the signal between base and emitter is not to exceed 5 mV.

**5.130** For the common-emitter amplifier shown in Fig. P5.130, let \( V_{\text{CC}} = 9 \, \text{V}, R_L = 27 \, \text{kΩ}, R_C = 15 \, \text{kΩ}, R_1 = 2 \, \text{kΩ} \), and \( R_2 = 2.2 \, \text{kΩ} \). The transistor has \( \beta = 100 \) and \( V_T = 100 \, \text{V}. \)
CHAPTER 5 BIPOLAR JUNCTION TRANSISTORS (BJTs)

5.131 Using the topology of Fig. P5.130, design an amplifier to operate between a 10-kΩ source and a 2-kΩ load with a gain $v_o/v_{in}$ of $-8$ V/V. The power supply available is 9 V. Use an emitter current of approximately 2 mA and a current of about one-tenth that in the voltage divider that feeds the base, with the dc voltage at the base about one-third of the supply. The transistor available has $V_{CE(sat)} = 2$ V, $V_{CC} = 9$ V, and $V_{BE} = 100$ V. Use standard 5%-resistance values, and specify the values of $R_1, R_2, R_E, R_L, R_F$, and $R_{in}$ for the input resistance of the amplifier and give the values of all its components. Neglect $v_{BE}$ and $v_{CE(sat)}$.

Comment.

5.133 Consider the CE amplifier circuit of Fig. 5.60(a). It is required to design the circuit (i.e., find values for $R_E, R_L, R_F$) to meet the following specifications:

(a) $R_L = 5$ kΩ.
(b) the dc voltage drop across $R_E$ is approximately 0.5 V.
(c) the open-circuit voltage gain from base to collector is the maximum possible, consistent with the requirement that the collector voltage never falls by more than approximately 0.5 V below the base voltage with the signal between base and emitter being as high as 5 mV.

Assume that $v_s$ is a sinusoidal source, the available supply $V_{CC} = 5$ V, and the transistor has $\beta = 100$ and a very large Early voltage. Use standard 5%-resistance values, and specify the value of $I$ to one significant digit. What base-to-collector open-circuit voltage gain does your design provide? If $R_L = 10$ kΩ, what is the overall voltage gain?

5.134 In the circuit of Fig. P5.134, $v_s$ is a small sine-wave signal with zero average. The transistor $\beta$ is 100.

(a) Find the value of $R_E$ to establish a dc emitter current of about 0.5 mA.
(b) Find $R_L$ to establish a dc collector voltage of about +5 V.
(c) For $R_L = 10$ kΩ and the transistor $\beta = 200$, draw the small-signal equivalent circuit of the amplifier and determine its overall voltage gain.

5.135 The amplifier of Fig. P5.135 consists of two identical common-emitter amplifiers connected in cascade. Observe that the input resistance of the second stage, $R_{in2}$, constitutes the load resistance of the first stage.

(a) For $V_{CC} = 15$ V, $R_L = 100$ kΩ, $R_{E1} = 47$ kΩ, $R_{E2} = 3.9$ kΩ, $R_L = 6.8$ kΩ, and $\beta = 100$, determine the dc collector current and collector voltage of each transistor.
(b) Draw the small-signal equivalent circuit of the entire amplifier and give the values of all its components. Neglect $v_{BE}$ and $v_{CE(sat)}$.
(c) Find $R_{in1}$ and $v_{in1}$ for $R_L = 5$ kΩ.
(d) Find $R_{in2}$ and $v_{in2}$.
(e) For $R_L = 2$ kΩ, find $v_{in2}$.
(f) Find the overall voltage gain $v_o/v_{in}$. 

FIGURE P5.130

FIGURE P5.134
5.136 In the circuit of Fig. P5.136, $v_s$ is a small sine-wave signal. Find $R_{in}$ and the gain $\beta = 100$. If the amplitude of the signal $v_s$ is to be limited to 5 mV, what is the largest signal at the input? What is the corresponding signal at the output?

5.137 The BJT in the circuit of Fig. P5.137 has $\beta = 100$.
(a) Find the dc collector current and the dc voltage at the collector.
(b) Replacing the transistor by its T model, draw the small-signal equivalent circuit of the amplifier. Analyze the resulting circuit to determine the voltage gain $v_o/v_i$.
(c) What is the ratio of maximum to minimum voltage gain obtained without $R_e$?
(d) What value of $R_e$ should be used to limit the ratio of maximum to minimum gain to 1.2?
(e) If the $R_e$ found in (b) is used, by what factor is the gain reduced (compared to the case without $R_e$) for a BJT with a nominal $\beta$?
5.139 Consider the CB amplifier of Fig. 5.62 with $R_L = 10 \, \text{k}\Omega$, $R_C = 10 \, \text{k}\Omega$, $V_{CC} = 10 \, \text{V}$, and $R_s = 100 \, \text{Ω}$. To what value must $I_e$ be set in order that the input resistance at $E$ is equal to that of the source (i.e., 100 Ω)? What is the resulting voltage gain from the source to the load? Assume $\alpha \approx 1$.

**D5.140** Consider the CB amplifier of Fig. 5.62(a) with the collector voltage signal coupled to a 1-kΩ load resistance through a large capacitor. Let the power supplies be ±5 V. The source has a resistance of 50 Ω. Design the circuit so that the amplifier input resistance is matched to that of the source and the output signal swing is as large as possible with relatively low distortion ($v_b$ limited to 10 mV). Find $I_e$ and $R_C$ and calculate the overall voltage gain obtained and the output signal swing. Assume $\alpha \approx 1$.

5.141 For the circuit in Fig. P5.141, find the input resistance $R_i$ and the voltage gain $v_o/v_s$. Assume that the source provides a small signal $v_s$ and that $\beta = 100$.

![FIGURE P5.141](image)

**FIGURE P5.141**

5.142 Consider the emitter follower of Fig. 5.63(a) for the case $I_e = 1 \, \text{mA}$, $\beta = 100$, $V_s = 100 \, \text{V}$, $R_p = 20 \, \text{k}\Omega$, and $R_C = 1 \, \text{k}\Omega$.

(a) Find $R_{in}$, $v_o/v_s$, and $v_e/v_s$.

(b) If $v_s$ is a sine-wave signal, to what value should its amplitude be limited in order that the transistor remains conducting at all times? For this amplitude, what is the corresponding amplitude across the base-emitter junction?

(c) If the signal amplitude across the base-emitter junction is to be limited to 10 mV, what is the corresponding amplitude of $v_e$ and of $v_s$?

(d) Find the open-circuit voltage gain $v_o/v_s$ and the output resistance. Use these values to determine the value of $v_e/v_s$ obtained with $R_C = 500 \, \text{Ω}$.

5.143 For the emitter-follower circuit shown in Fig. P5.143, the BJT is specified to have $\beta$ values in the range of 40 to 200 (a distressing situation for the circuit designer). For the two extreme values of $\beta$ ($\beta = 40$ and $\beta = 200$), find:

(a) $I_e$, $V_o$, and $V_B$

(b) the input resistance $R_i$

(c) the voltage gain $v_o/v_s$

![FIGURE P5.143](image)

5.144 In the emitter follower in Fig. P5.144, the signal source is directly coupled to the transistor base. If the dc component of $v_s$ is zero, find the dc emitter current. Assume $\beta = 100$. Neglecting $r_o$, find $R_{out}$, the voltage gain $v_o/v_s$, the current gain $i_o/i_s$, and the output resistance $R_{out}$.

![FIGURE P5.144](image)

5.145 In the emitter follower of Fig. 5.63(a), the signal source is directly coupled to the base. Thus, $C_{bc}$ and $R_p$ are eliminated. The source has $R_s = 10 \, \text{k}\Omega$ and a dc component of zero. The transistor has $\beta = 100$ and $V_B = 125 \, \text{V}$. The bias current $I_b = 2.5 \, \text{mA}$, and $V_{CC} = 5 \, \text{V}$. What is the output resistance
5.146 The emitter follower of Fig. 5.63(a), when driven from a 10-kΩ source, was found to have an open-circuit voltage gain of 0.99 and an output resistance of 200 Ω. The output resistance increased to 300 Ω when the source resistance was increased to 20 kΩ. Find the overall voltage gain when the follower is driven by a 30-kΩ source and loaded by a 1-kΩ resistor. Assume \( r_e \) is very large.

**5.147** For the circuit in Fig. P5.147, called a *bootstrapped* follower:

(a) Find the dc emitter current and \( g_m, r_e, \) and \( r_\pi \). Use \( \beta = 100. \)
(b) Replace the BJT with its T model (neglecting \( r_e \)), and analyze the circuit to determine the input resistance \( R_{in} \) and the voltage gain \( \frac{v_o}{v_s} \).
(c) Repeat (b) for the case when capacitor \( C_B \) is open-circuited. Compare the results with those obtained in (b) to find the advantages of bootstrapping.

**FIGURE P5.147**

**5.148** For the follower circuit in Fig. P5.148 let transistors \( Q_1 \) and \( Q_2 \) have \( \beta = 50 \) and \( \beta = 100 \), and neglect the effect of \( r_e \). Use \( V_{BE} = 0.7 \) V.

(a) Find the dc emitter current of \( Q_1 \) and \( Q_2 \). Also, find the dc voltages \( V_{CE} \) and \( V_{CB} \).
(b) If a load resistance \( R_L = 2 \) kΩ is connected to the output terminal, find the output resistance of the base to the emitter of \( Q_2, \frac{v_o}{v_s} \), and find the input resistance \( R_{in} \) looking into the base of \( Q_2 \). (Hint: Consider \( Q_2 \) as an emitter follower fed by a voltage \( v_{b2} \) at its base.)
(c) Replacing \( Q_2 \) with its input resistance \( R_{in} \) found in (b), analyze the circuit of emitter follower \( Q_1 \) to determine its input resistance \( R_{in} \), and the gain from its base to its emitter, \( \frac{v_o}{v_s} \).
(d) If the circuit is fed with a source having a 100-kΩ resistance, find the transmission to the base of \( Q_2, \frac{v_o}{v_s} \).
(e) Find the overall voltage gain \( \frac{v_o}{v_s} \).

**FIGURE P5.148**

SECTION 5.8: THE BJT INTERNAL CAPACITANCES AND HIGH-FREQUENCY MODEL

5.149 An npn transistor is operated at \( I_C = 0.5 \) mA and \( V_{CEA} = 2 \) V. It has \( \beta = 100, V_B = 50 \) V, \( r_e = 30 \) pF, \( C_{je} = 20 \) pF, \( C_{\pi} = 0.75 \) V, \( m_B = 0.5 \), and \( \tau_F = 0.1 \) Ω. Sketch the complete hybrid-\( \pi \) model, and specify the values of all its components. Also, find \( f_T \).

5.150 Measurement of \( h_{fe} \) of an npn transistor at 500 MHz shows that \( |h_{fe}| = 2.5 \) at \( I_C = 0.2 \) mA and \( 11.6 \) at \( I_C = 1 \) mA. Furthermore, \( C_{\pi} \) was measured and found to be 0.05 pF. Find \( f_T \) at each of the two collector currents used. What must \( V_C \) and \( C_B \) be?

5.151 A particular BJT operating at \( I_C = 2 \) mA has \( C_{je} = 1 \) pF, \( C_{\pi} = 10 \) pF, and \( \beta = 150 \). What are \( f_T \) and \( f_B \) for this situation?

5.152 For the transistor described in Problem 5.151, \( C_B \) includes a relatively constant depletion-layer capacitance of 2 pF.
5.153 A particular small-geometry BJT has $f_T$ of 5 GHz and $C_\pi = 0.1 \, \mu F$ when operated at $I_c = 0.5 \, mA$. What is $\beta_0$ in this situation? Also, find $f_B$. For $f = 150$, find $r_e$ and $f_o$.

5.154 For a BJT whose unity-gain bandwidth is 1 GHz and $\beta = 200$, at what frequency does the magnitude of $h_{re}$ become 20? What is $f_T$?

5.155 For a sufficiently high frequency, measurement of the complex input impedance of a BJT having (ac) grounded emitter and collector yields a real part approximating the complex input impedance of a BJT having (ac) grounded base.

5.156 Complete the table entries above for transistors (a) through (g), under the conditions indicated. Neglect $r_e$.

5.157 A designer wishes to investigate the effect of changing the bias current on the midband gain and high-frequency response of the CE amplifier considered in Example 5.18. Let $I_e$ be doubled to 2 mA, and assume that $r_e$ and $f_o$ remain unchanged at 100 MHz and 800 MHz, respectively. To keep the node voltages nearly unchanged, the designer reduces $R_b$ and $R_C$ by a factor of 2 to 50 kΩ and 4 kΩ, respectively. Assume $r_e = 50 \, \Omega$, and recall that $V_{be} = 100 \, \text{V}$ and that $C_\pi$ remains constant at 1 pF. As before, the amplifier is fed with a source having $R_{in} = 5 \, \text{kΩ}$ and feeds a load $R_L = 5 \, \text{kΩ}$. Find the new values of $A_{in}$, $f_o$, and the gain–bandwidth product, $f_{max}$. Comment on the results. Note that the price paid for whatever improvement in performance is achieved is an increase in power. By what factor does the power dissipation increase?

5.158 The purpose of this problem is to investigate the high-frequency response of the CE amplifier when it is fed with a relatively large source resistance $R_{in}$. Refer to the amplifier in Fig. 5.71(a) and to its high-frequency equivalent-circuit model and the analysis shown in Fig. 5.72. Let $R_L > R_{in}$, $r_e < R_{in}$, $R_{ro} > r_e$, and $R_L > R_{ro}$. For $f = 100$, find the midband gain and $f_o$ for the two cases $R_C = 25 \, \text{kΩ}$ and $R_C = 2.5 \, \text{kΩ}$. On the same coordinates, sketch Bode plots for the gain magnitude versus frequency for the two cases. What $f_o$ is obtained when the gain is unity? What value of $R_C$ corresponds?

5.159 Consider the common-emitter amplifier of Fig. P5.159 under the following conditions: $R_{in} = 5 \, \text{kΩ}$, $R_L = 5 \, \text{kΩ}$, $R_C = 22 \, \text{kΩ}$, $R_{ro} = 3.9 \, \text{kΩ}$, $R_e = 4.7 \, \text{kΩ}$, $R_f = 5.6 \, \text{kΩ}$, $V_{cc} = 5 \, \text{V}$. The dc emitter current can be shown to be $I_e = 0.3 \, \text{mA}$, at which $\beta = 120$, $r_e = 300 \, \text{kΩ}$, and $r_o = 50 \, \text{Ω}$. Find the input resistance $R_{in}$ and the midband gain $A_{in}$. If the transistor is specified to have $f_o = 700 \, \text{MHz}$ and $C_\pi = 1 \, \text{pF}$, find the upper 3-dB frequency $f_{max}$.
5.160 For a version of the CE amplifier circuit in Fig. P5.159, \( R_{C} = 10 \, \text{k}\Omega, R_{b} = 68 \, \text{k}\Omega, R_{e} = 27 \, \text{k}\Omega, R_{c} = 2.2 \, \text{k}\Omega, R_{L} = 4.7 \, \text{k}\Omega, \) and \( R_{F} = 10 \, \text{k}\Omega. \) The collector current is 0.8 mA, \( f_{j} = 1 \, \text{GHz}, \) and \( C_{j} = 0.8 \, \text{pF}. \) Neglecting the effect of \( r_{e} \) and \( r_{C} \), find the midband voltage gain and the upper 3-dB frequency, \( f_{u}. \)

5.161 The amplifier shown in Fig. P5.161 has \( R_{C} = R_{b} = 1 \, \text{k}\Omega, R_{e} = 1 \, \text{k}\Omega, R_{c} = 47 \, \text{k}\Omega, r_{e} = 100, C_{j} = 0.8 \, \text{pF}, \) and \( f_{j} = 600 \, \text{MHz}. \) Find the midband voltage gain and the upper 3-dB frequency, \( f_{u}. \)

5.162 Refer to Fig. P5.162. Utilizing the BJT high-frequency hybrid-\( \pi \) model with \( r_{e} = 0 \) and \( r_{C} = \infty, \) derive an expression for \( Z(s) \) as a function of \( r_{b}, r_{e}, C_{b}, \) and \( C_{e}. \) Find the frequency at which the impedance has a phase angle of 45° for the case in which the BJT has \( f_{j} = 400 \, \text{MHz} \) and the bias current is relatively high. What is the frequency when the bias current is reduced so that \( C_{b} = C_{e}? \) Assume \( a = 1. \)

5.163 For the amplifier in Fig. P5.159, whose component values were specified in Problem 5.159, let \( C_{1} = C_{2} = 1 \, \mu\text{F}, \) and \( C_{j} = 10 \, \text{pF}. \) Find the break frequencies \( f_{P}, f_{T}, f_{L}, \) and \( f_{C} \) resulting for \( C_{1}, C_{2}, \) and \( C_{j}. \) respectively. Note that \( R_{L} \) has to be taken into account in evaluating \( f_{C}. \) Hence, estimate the value of the lower 3-dB frequency, \( f_{L}. \)

5.164 For the amplifier described in Problem 5.163, design the coupling and bypass capacitors for a lower 3-dB frequency of 100 Hz. Design so that the contribution of each \( C_{1} \) and \( C_{j} \) to determining \( f_{L} \) is only 5%.

5.165 Consider the circuit of Fig. P5.159. For \( R_{C} = 10 \, \text{k}\Omega, R_{b} = R_{e} \equiv R_{j} = 10 \, \text{k}\Omega, r_{e} = 100, r_{C} = 1 \, \text{k}\Omega, \beta = 100, \) and \( R_{L} = 1 \, \text{k}\Omega, \) what is the ratio \( C_{j}/C_{C}, \) that makes its contributions to the determination of \( f_{C} \) equal?

5.166 For the common-emitter amplifier of Fig. P5.166, neglect \( r_{b} \) and \( r_{e}, \) and assume the current source to be ideal.

5.167 The BJT common-emitter amplifier of Fig. P5.167 includes an emitter degeneration resistance \( R_{b}. \)

(a) Assuming \( a = 1, \) neglecting \( r_{b} \) and \( r_{e}, \) and assuming the current source to be ideal, derive an expression for the small-signal voltage gain \( A_{v} \equiv V_{o}/V_{i}. \) Hence find the midband gain, \( A_{M}, \) and the lower 3-dB frequency, \( f_{L}. \)

(b) Show that including \( R_{b} \) reduces the magnitude of \( A_{M} \) by a certain factor. What is this factor?

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**FIGURE P5.161**

**FIGURE P5.162**

**FIGURE P5.163**

**FIGURE P5.164**

**FIGURE P5.165**
(c) Show that including $R_e$ reduces $I_c$ by the same factor as in (b) and thus one can use $R_e$ to trade-off gain for bandwidth. (d) For $I_c = 1\, \text{mA}$, $R_e = 10\, \text{k}\Omega$, and $C_p = 100\, \text{nF}$, find $A_{cm}$ and $f_c$ with $R_e = 0$. Now find the value of $R_e$ that lowers $I_c$ by a factor of 5. What will the gain become?

For the circuit in Fig. P5.171, consider the application of inputs of 5 V and 0.2 V to X and Y in any combination, and find the output voltage for each combination. Tabulate your results. How many input combinations are there? What happens when both inputs are low? This is a logic gate that implements the NOR function: $Z = X + Y$.
assume that prior to $t = 0$, the transistor is off and $v_{OH} = V_{CC}$. Then, at $t = 0$, let the input rise to the high level, and assume that the transistor turns on instantaneously. Note that neglecting the delay time of the transistor is unrealistic but will help us concentrate on the effect of the load capacitance $C$.

Now, because $C$ cannot discharge instantaneously, the transistor cannot saturate immediately. Rather, it will operate in the active mode, and its collector will supply a constant current of $\beta (V_{CC} - V_{BE})/R_C$. Find the Thévenin equivalent circuit for discharging the capacitor, and show that the voltage will fall exponentially, starting at $V_{CC}$ and heading toward a large negative voltage of $[V_{CC} - \beta (V_{CC} - V_{BE})R_C/R_B]$. Find an expression for $v_{OH}(t)$. This exponential discharge will stop when $v_{OH}$ reaches $V_{OH}$ and the transistor saturates. Calculate the value of $t_{PHL}$, which in this case is the time for $v_{OH}$ to fall to $\left(\frac{V_{OH} + V_{BE}}{2}\right)$. Use $V_{CC} = 5 \text{ V}$, $V_{BE} = 0.2 \text{ V}$, $V_{CE} = 0.7 \text{ V}$, $R_B = 10 \text{ k}\Omega$, $R_C = 1 \text{ k}\Omega$, $\beta = 50$, and $C = 10 \text{ pF}$. If you have solved Problem 5.172, compare the value of $t_{PHL}$ to that of $t_{PLH}$ found there, and find the inverter delay, $t_p$. (Hint: The step response of $RC$ circuits is reviewed in Section 1.7 and in greater detail in Appendix F).